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SIMATIC

Automation System S7-400 CPU Specifications

Reference Manual

This manual is part of the documentation package with the order number
6ES7398-8AA03-8BA0

Edition 12/2002
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Safety Guidelines

This manual contains notices intended to ensure personal safety, as well as to protect the products and connected equipment against damage. These notices are highlighted by the symbols shown below and graded according to severity by the following texts:

Danger

indicates that death, severe personal injury or substantial property damage will result if proper precautions are not taken.

Warning

indicates that death, severe personal injury or substantial property damage can result if proper precautions are not taken.

Caution

indicates that minor personal injury can result if proper precautions are not taken.

Caution

indicates that property damage can result if proper precautions are not taken.

Notice

draws your attention to particularly important information on the product, handling the product, or to a particular part of the documentation.

Qualified Personnel

Only **qualified personnel** should be allowed to install and work on this equipment. Qualified persons are defined as persons who are authorized to commission, to ground and to tag circuits, equipment, and systems in accordance with established safety practices and standards.

Correct Usage

Note the following:

Warning

This device and its components may only be used for the applications described in the catalog or the technical description, and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens.

This product can only function correctly and safely if it is transported, stored, set up, and installed correctly, and operated and maintained as recommended.

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Disclaim of Liability

We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

Technical data subject to change.

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Preface

Purpose of the Manual

The manual contains reference information on operator actions, descriptions of functions and technical specifications of the central processing units, power supply modules and interface modules of the S7-400.

How to configure, assemble and wire these modules (and other) in an S7-400 system is described in the installation manuals for each system.

Required Basic Knowledge

You will need general knowledge of automation to understand this manual.

Target Group

This manual is aimed at people with the required qualifications to commission, operate and maintain the products described.

Scope of this Manual

The manual applies to the S7-400 automation system.

Changes Since the Previous Version

This manual describes S7 CPUs with firmware version 3.1.

Certification

The SIMATIC S7-400 product range has the following certificates:

- Underwriters Laboratories, Inc.: UL 508 (Industrial Control Equipment)
- Canadian Standards Association: CSA C22.2 Number 142, tested (Process Control Equipment)
- Factory Mutual Research: Approval Standard Class Number 3611.

You can find details on the certificates and approvals in section 1.1, Standards and Certificates, of the “Module Specifications” reference manual.

CE Labeling

The SIMATIC S7-400 product range complies with the requirements and protection objectives of the following EU directives:

- EC low voltage directive 73/23/EEC
- EC electromagnetic compatibility directive 89/336/EEC

C-Tick Mark

The SIMATIC S7-400 product range complies with the requirements of the AS/NZS 2064 standard (Australia and New Zealand).

Standards

The SIMATIC S7-400 product range complies with the requirements and criteria of the IEC 61131-2.

Place of this Documentation in the Information Environment

This manual is part of the documentation package for S7-400, M7-400.

System	Documentation Package
S7-400/M7-400	• *S7-400, M7-400 Programmable Controller*; *Hardware and Installation* • *S7-400, M7-400 Programmable Controllers; Module Specifications* • *Automation System S7-400; CPU Data* • *S7-400 Instruction List*

Navigating

The manual offers the following access aids to make it easy for you to find specific information quickly:

- At the start of the manual you will find a complete table of contents and a list of the diagrams and tables that appear in the manual.
- An overview of the contents of each section is provided in the left column on each page of each chapter.
- You will find a glossary in the appendix at the end of the manual. The glossary contains definitions of the main technical terms used in the manual.
- At the end of the manual you will find a comprehensive index which gives you rapid access to the information you need.

Note

In order to program and commission an S7-400 you require
STEP 7 V52 as well as the following manuals or manual packages:

Manual/ Manual Package	Chapter Overview
Standard Software for S7 and M7 STEP 7 Basic Information	• Installing and starting up STEP 7 on a programming device / PC • Working with STEP 7 with the following contents: Managing projects and files Configuring and assigning parameters to the S7-400 configuration Assigning symbolic names for user programs Creating and testing a user program in STL/LAD Creating data blocks Configuring the communication between two or more CPUs Loading, storing and deleting user programs in the CPU / programming device Monitoring and controlling user programs Monitoring and controlling the CPU • Guide for efficiently implementing the programming task with the programming device / PC and STEP 7 • How the CPUs work (for example, memory concept, access to inputs and outputs, addressing, blocks, data management) • Description of STEP 7 data management • Using data types of STEP 7 • Using linear and structured programming • Using block call instructions • Using the debug and diagnostic functions of the CPUs in the user program (for example, error OBs, status word)
STEP 7 Reference Information *Statement List (STL) for S7-300 and S7-400* *Ladder Logic (LAD) for S7-300 and S7-400* *Function Block Diagram (FBD) for S7-300 and S7-400* *System and Standard Functions*	• Basic procedure for working with STL, LAD, or FBD (for example, structure of STL, LAD, or FBD, number formats, syntax) • Description of all instructions in STEP 7 (with program examples) • Description of the various addressing methods in STEP 7 (with examples) • Description of all functions integrated in the CPUs • Description of the internal registers in the CPU • Description of all system functions integrated in the CPUs • Description of all organization blocks integrated in the CPUs
Manual *PG 7xx*	• Description of the programming device hardware • Connecting a programming device to various devices • Starting up a programming device

Recycling and Disposal

The S7-400 is low in contaminants and can therefore be recycled. To recycle and dispose of your old device in an environment-friendly manner, please contact a disposal company certified for disposal of electronic waste.

Further Support

If you have any technical questions, please get in touch with your Siemens representative or agent responsible.

`http://www.siemens.com/automation/partner`

Training Centers

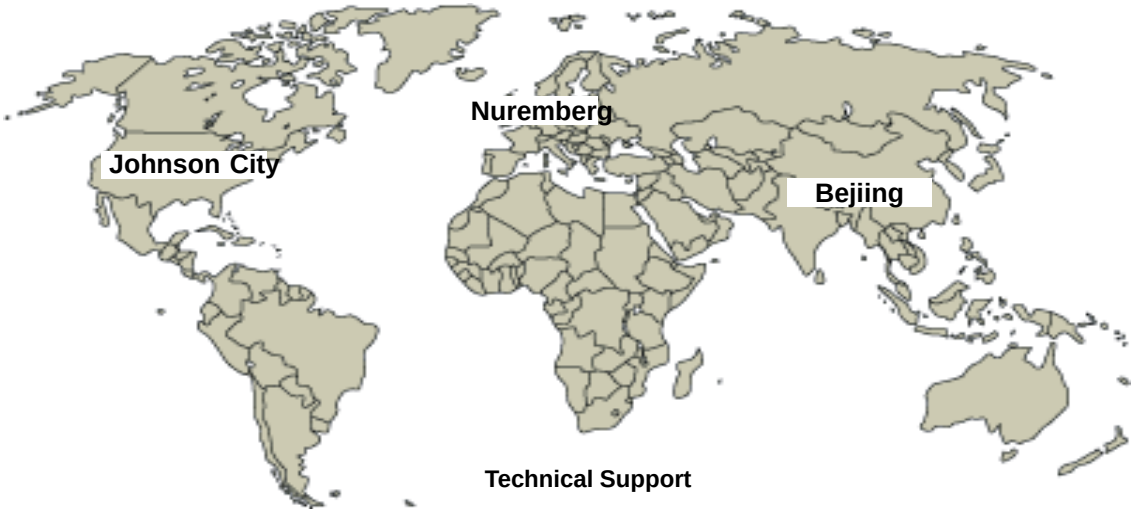
We offer a number of courses to help you become familiar with the SIMATIC S7 programmable logic controller. Please contact your regional training center or our central training center in D 90327 Nuremberg, Germany for details:

Phone: +49 (911) 895-3200.

Internet: `http://www.sitrain.com`

A&D Technical Support

Available 24 hours a day, worldwide:



Worldwide (Nuremberg) **Technical Support** Local time: 0:00 to 24:00 / 365 days Phone: +49 (0) 180 5050-222 Fax: +49 (0) 180 5050-223 E-Mail: adsupport@ siemens.com GMT: +1:00		
Europe / Africa (Nuremberg) **Authorization** Local time: Mo. - Fr. 8:00 am to 5:00 pm Phone: +49 (0) 180 5050–222 Fax: +49 (0) 180 5050-223 E-Mail: adsupport@ siemens.com GMT: +1:00	**United States** (Johnson City) **Technical Support and Authorization** Local time: Mo. - Fr. 8:00 am to 5:00 pm Phone: +1 (0) 423 262 2522 Fax: +1 (0) 423 262 22 89 E-mail: simatic.hotline@ sea.siemens.com GMT: –5:00	**Asia / Australia** (Bejiing) **Technical Support and Authorization** Local time: Mo. - Fr. 8:00 am to 5:00 pm Phone: +86 10 64 75 75 75 Fax: +86 10 64 74 74 74 E-mail: adsupport.asia@ siemens.com GMT: +8:00
The languages of the SIMATIC Hotlines and the authorization hotline are generally German and English.		

Service & Support in the Internet

In addition to our documentation, we also offer you the benefit of all our knowledge on the Internet.

`http://www.siemens.com/automation/service&support`

There you will find:

- A newsletter with all the latest information on your products
- Knowledge Manager to locate the documentation you require
- A forum in which users and specialists throughout the world exchange their experiences
- Your local contact person for Automation & Drives using our contact database
- Information about our on-site service, repairs, spare parts and much more is available under the heading “Service”.

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Structure of a CPU 41x

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Chapter Overview

1.1 Controls and Indicators of the CPUs

Controls and Indicators of the CPU 412-1

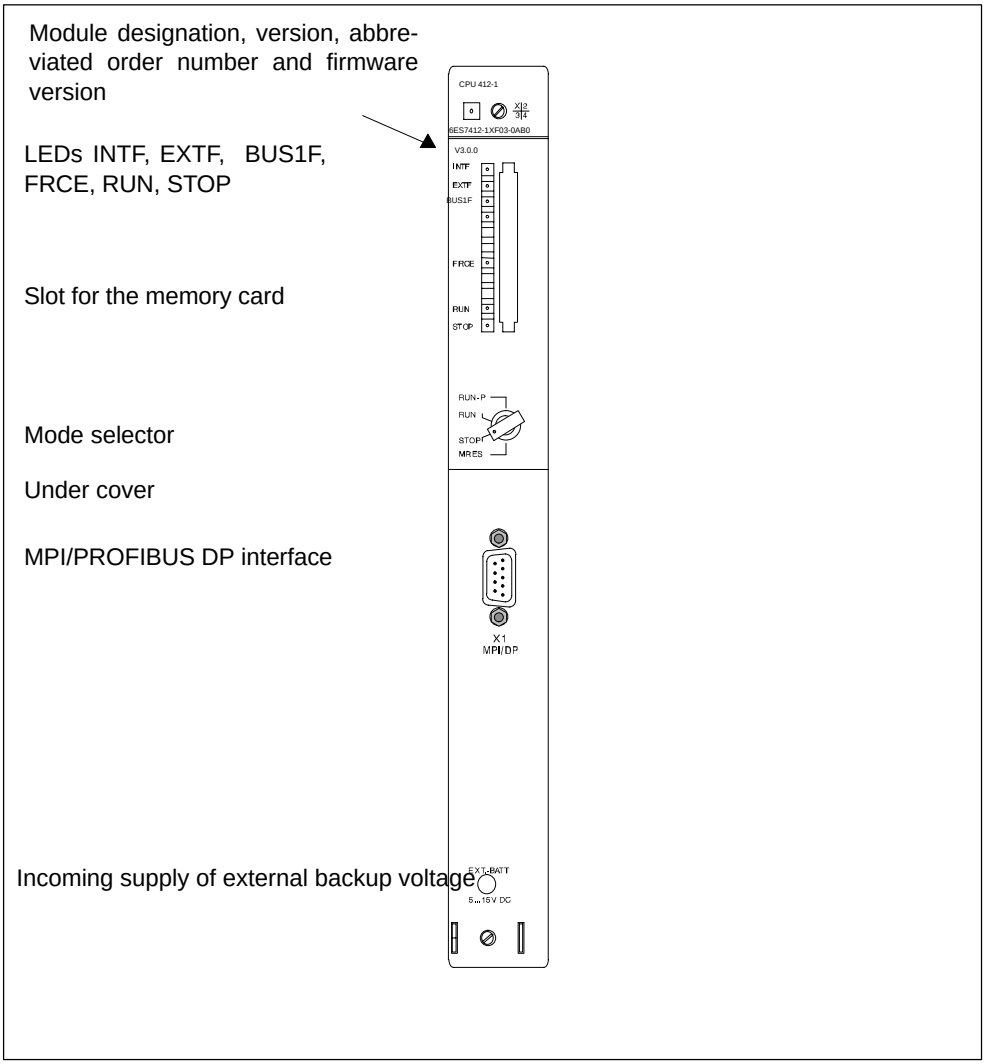


Figure 1-1 Layout of the Controls and Indicators of the CPU 412-1

Controls and Indicators of the CPU 41x-2

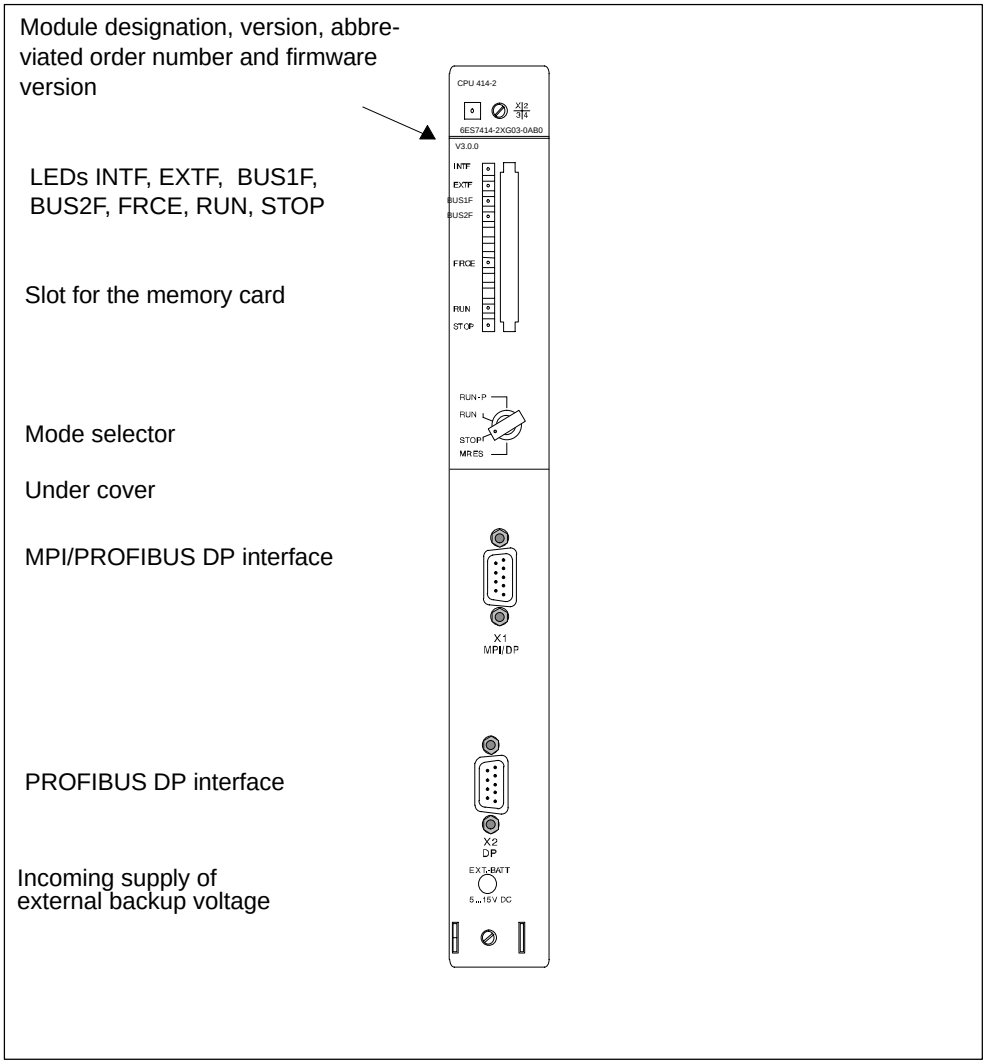


Figure 1-2 Layout of the Controls and Indicators of the CPU 41x-2

Controls and Indicators of the CPU 41x-3

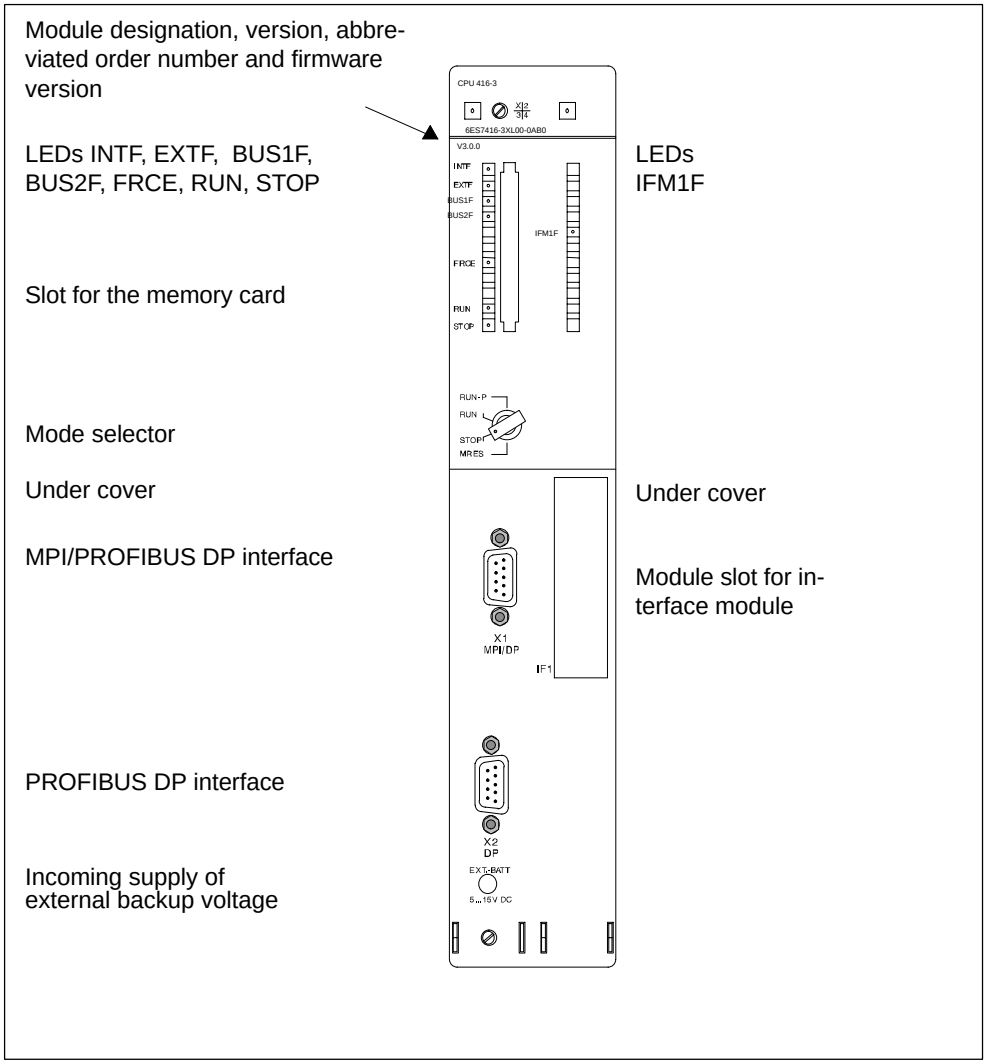


Figure 1-3 Layout of the Controls and Indicators of the CPU 41x-3

Controls and Indicators of the CPU 417-4

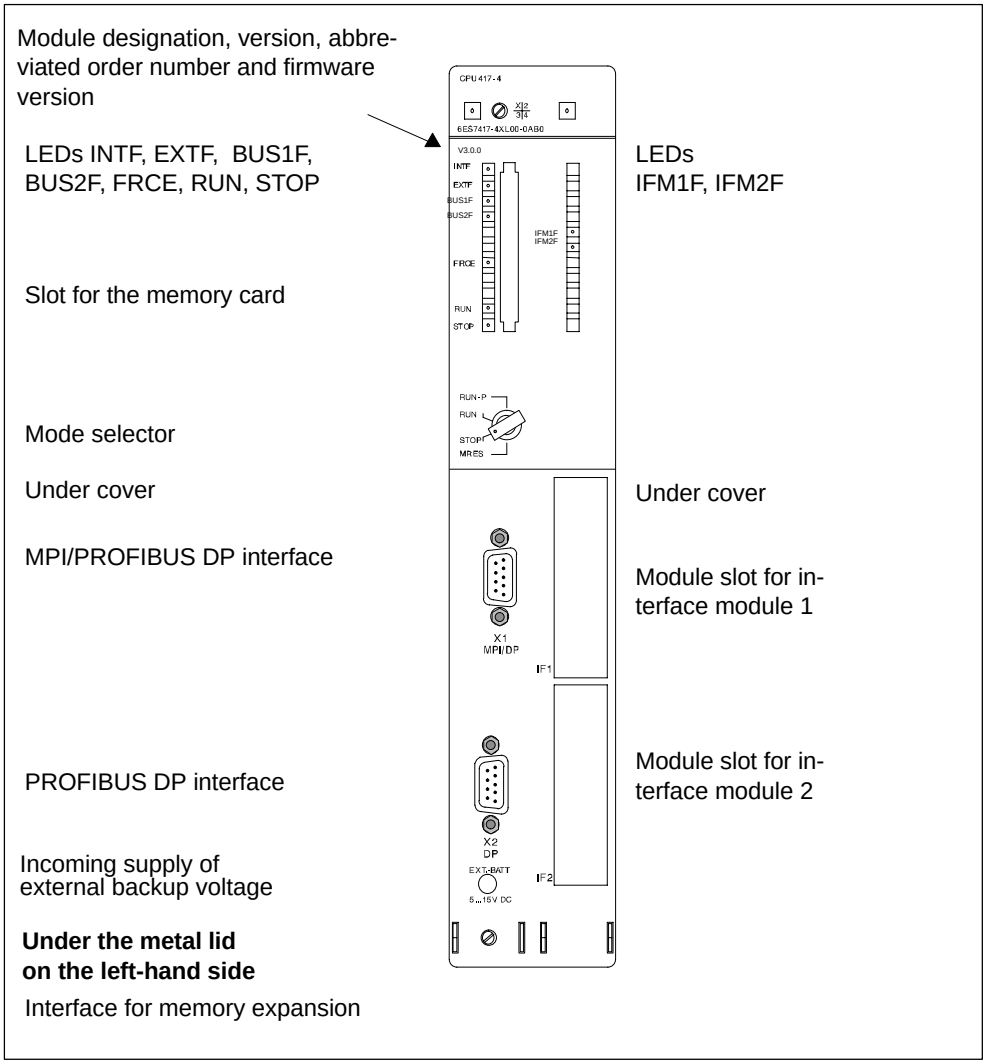


Figure 1-4 Layout of the Controls and Indicators of the CPU 417-4

LEDs

Table 1-1 gives you an overview of the LEDs on the individual CPUs.

Section 1.2 describes the states and errors indicated by these LEDs.

Table 1-1 LEDs of the CPUs

LED	Color	Meaning	In CPU			
			412-1	412-2 414-2 416-2	414-3 416-3	417-4
INTF	red	Internal fault	x	x	x	x
EXTF	red	External fault	x	x	x	x
FRCE	yellow	Active force request	x	x	x	x
RUN	green	RUN mode	x	x	x	x
STOP	yellow	STOP mode	x	x	x	x
BUS1F	red	Bus fault at MPI/PROFIBUS DP interface 1	x	x	x	x
BUS2F	red	Bus fault at PROFIBUS DP interface 2	–	x	x	x
IFM1F	red	Error at interface submodule 1	–	–	x	x
IFM2F	red	Error at interface submodule 2	–	–	–	x

Mode Selector

You can use the mode selector to select the current operating mode of the CPU. The mode selector is a key switch with four switching positions. You can use different protection levels and limit any program changes or startup options (STOP to RUN transition) to a certain group of people.

Section 1.4 describes the functions of the mode selector and the protection levels of the CPUs.

Slot for Memory Cards

You can insert a memory card in this slot.

There are two types of memory card:

- RAM cards

  You can expand the load memory of a CPU with the RAM card.

- FLASH cards

  You can use the FLASH card to store your user program and your data so that they are failproof (even without a backup battery). You can either program the FLASH card on the programming device or in the CPU. The FLASH card also expands the load memory of the CPU.

  You can find a detailed description of the memory cards in Chapter 1.5.

Slot for Interface Modules

You can insert one interface module (IF module) for each CPUs 41x-3 and 41x-4 in this slot.

Interface for Memory Expansion

CPU 417-4 also features interfaces for memory expansion. These make it possible to expand the working memory. (See *"S7-400, M7-400 Programmable Controllers,* Hardware and Installation")

MPI/DP interface

You can connect the following devices to the MPI of the CPU, for example:

- Programming devices
- Operation and monitoring devices
- Additional S7-400 or S7-300 controllers (see Section 1.6).

Use the bus connector with an angular outgoing cable (see the Installation manual, Chapter 7)

You can also configure the MPI interface as a DP master and use it as a PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP interface

You can connect the distributed I/O, programming devices/OPs and additional DP master stations to the PROFIBUS DP interface.

Incoming Supply of External Backup Voltage at the “EXT.-BATT.” Socket

You can use one or two backup batteries – depending on the module type – in the power supply modules of the S7-400 to do the following:

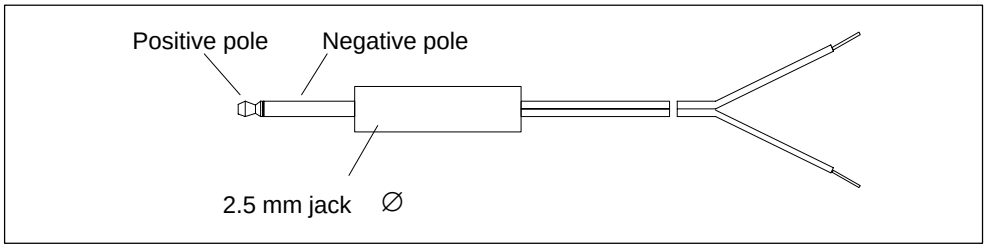
- Provide backup power for the user program you have stored in RAM.
- Maintain memory bits, times, counts and system data as well as data in variable data blocks.
- Provide backup power for the internal clock.

You can achieve the same backup power by connecting a voltage between 5 V and 15 V DC to the “EXT.-BATT.” socket of the CPU.

The “EXT.-BATT.” input has the following features:

- Reverse polarity protection
- A short-circuit current limit of 20 mA

You need a cable with a 2.5 mm ∅ jack to connect power to the “EXT.-BATT” socket, as shown in the following illustration. Note the polarity of the jack.



Note

You will require the external incoming supply at the “EXT.-BATT.” socket if you replace a power supply module and want to provide a backup supply for the user program stored in RAM and the data mentioned above while the module is being replaced.

1.2 Monitoring Functions of the CPU

Monitoring and Error Messages

The CPU hardware and the operating system have monitoring functions that ensure that the system functions correctly and that there is a defined response in the event of an error. A number of errors will also produce a response from the user program.

The following table gives you an overview of possible errors, their causes and the responses of the CPU.

Type of Fault/Error	Cause of Fault	Response of the Operating System	Error LED
Clock pulse failure	Monitoring of the failure of the processor clock pulse System standstill	Disabling of the digital outputs by issuing the “OD” (Output Disable) signal	–
Access error	Module failure (SM, FM, CP)	”EXTF” LED lights up until the fault is acknowledged. In SMs: • OB 122 call • Entry in the diagnostic buffer • In the case of input modules: Entry of null for the date in the accumulator or the process image In the case of other modules: • OB 122 call	EXTF
Clock synchronous interrupt	Start a program synchronized to the DP clock	Call OB 61 to OB 64	–
Timing error	• The runtime of the user program (OB1 and all the interrupts and error OBs) exceeds the specified maximum cycle time. • OB request error • Overrun of the start information buffer • Time error interrupt • Re-enter RUN following CiR	”INTF” LED lights up until the fault is acknowledged. OB 80 call If the OB is not loaded: The CPU goes into STOP mode.	INTF
Power supply module error (not power failure)	In the central or distributed I/O rack: • At least one backup battery in the power supply module is empty. • The backup voltage is missing. • The 24 V supply to the power supply module has failed.	OB 81 call If the OB is not loaded: The CPU continues to run.	EXTF
Diagnostic Interrupt	An I/O module with interrupt capability reports a diagnostic interrupt.	OB 82 call If the OB is not loaded: The CPU goes into STOP mode.	EXTF
Remove/insert interrupt	Removal or insertion of an SM and insertion of an incorrect module type. The LED EXTF will not light up if the only inserted SM is removed from the CPU in STOP during default configuration. The LED lights up briefly when the SM is inserted again.	OB 83 call If the OB is not loaded: The CPU goes into STOP mode.	EXTF

Type of Fault/Error	Cause of Fault	Response of the Operating System	Error LED
Priority class error	• Priority class is called, but the corresponding OB is not available. • In the case of an SFB call: The instance DB is missing or defective. • Error during the updating of the process image	OB 85 call If the OB is not loaded: The CPU goes into STOP mode.	INTF EXTF
Failure of a rack/station	• Power failure in an expansion rack • Failure of a DP line • Failure of a coupling line: missing or defective IM, interrupted line)	OB 86 call If the OB is not loaded: The CPU goes into STOP mode.	EXTF
Communication error	• Status information cannot be entered in DB • Incorrect frame identifier • Frame length error • Error in the structure of the global data message • DB access error	OB 87 call If the OB is not loaded: The CPU goes into STOP mode.	INTF
Cancel processing	• Nesting depth exceeded for synchronous errors • Too many nested block calls (B stack) • Error allocating local data	Call OB 88 If the OB is not loaded: The CPU goes into STOP mode.	INTF
Programming error	Error in the machine code or in the user program: • BCD conversion error • Range length error • Range error • Alignment error • Write error • Timer number error • Counter number error • Block number error • Block not loaded	OB 121 call If the OB is not loaded: The CPU goes into STOP mode.	INTF
MC7 code error	Error in the compiled user program (e.g. impermissible OP code or jump over the end of the block)	CPU goes into STOP mode. Reboot or memory reset required.	INTF
Loss of clock	Clock was lost either because an OB 61 to 64 was not start due to higher priorities or because additional asynchronous bus loads suppressed the bus clock.	Call OB 61..64 at the next pulse.	INTF EXTF

There are also test and information functions available in each CPU that you can call up with STEP 7.

1.3 Status and Error LEDs

Status LEDs

The two RUN and STOP LEDs on the front panel of a CPU informs you of the currently active CPU operating status.

LED		Meaning
RUN	**STOP**	
H	D	CPU is in RUN state.
D	H	CPU is in STOP state. The user program is not processed. Restart and warm restart/reboot is possible. If the STOP status was triggered by an error, the error indication (INTF or EXTF) is also set.
B 2 Hz	B 2 Hz	CPU has the status DEFECT. The INTF, EXTF and FRCE LEDs also flash.
B 0.5 Hz	H	HALT status has been triggered by a test function.
B 2 Hz	H	A warm restart/reboot/restart has been triggered. It can take a minute or longer to execute the warm restart/reboot/restart depending on the length of the OB called. If the CPU still does not go into RUN, there might be an error in the system configuration.
x	B 0.5 Hz	Memory reset is requested by the CPU.
x	B 2 Hz	Memory reset is running.

D = LED is dark; H = LED lights up; B = LED flashes with the specified frequency;
x = LED status is irrelevant

Error Displays and Points to Note, All CPUs

The three LEDs INTF, EXTF and FRCE on the front panel of a CPU inform you about the errors and points to note during the execution of the user program.

LED			Meaning
INTF	**EXTF**	**FRCE**	
H	x	x	An internal has been detected (program or configuration error) or the CPU is performing a CiR.
x	H	x	An external error has been detected (in other words, the cause of the error cannot be traced back to the CPU module).
x	x	H	A force request is active.

H = LED lights up; x = LED status is irrelevant

The LEDs BUSF1 and BUSF2 indicate errors in connection with the MPI/DP interface and the PROFIBUS DP interface.

LED		Meaning
BUS1F	**BUS2F**	
H	x	An error has been detected at the MPI/DP interface.
x	H	An error has been detected at the PROFIBUS DP interface.
B	x	DP master: One or more slaves at PROFIBUS DP interface 1 are not replying. DP slave: not addressed by the DP master
x	B	DP master: One or more slaves at PROFIBUS DP interface 2 are not replying. DP slave: not addressed by the DP master

H = LED lights up; B = LED flashes; x = LED status is irrelevant

Error LEDs and Points to Note, CPU 41x-3 and 41x-4

The CPUs 41x-3 and 41x-4 continue to have the LED IFM1F and LEDs IFM1F and IFM2F. These indicate errors in connection with the first and second module interfaces.

LED		Meaning
IFM1F	**IFM2F**	
H	x	An error has been detected at module interface 1.
x	H	An error has been detected at module interface 2.
B	x	DP master: One or more slaves on the PROFIBUS DP interface module inserted in module slot 1 are not responding DP slave: not addressed by the DP master
x	B	DP master: One or more slaves on the PROFIBUS DP interface module inserted in module slot 2 are not responding DP slave: not addressed by the DP master

H = LED lights up; B = LED flashes; x = LED status is irrelevant

Diagnostic buffer

You can read out the exact cause of an error in STEP 7 (PLC –> Module Information) from the diagnostic buffer.

1.4 Mode Selector

Function of the Mode Selector

Using the mode selector, you can put the CPU in RUN/RUN-P or STOP mode or reset the memory of the CPU. STEP 7 offers further options for changing the mode.

Positions

The mode selector switch is designed as a keyswitch. Figure 1-5 illustrates the possible positions of the mode selector.

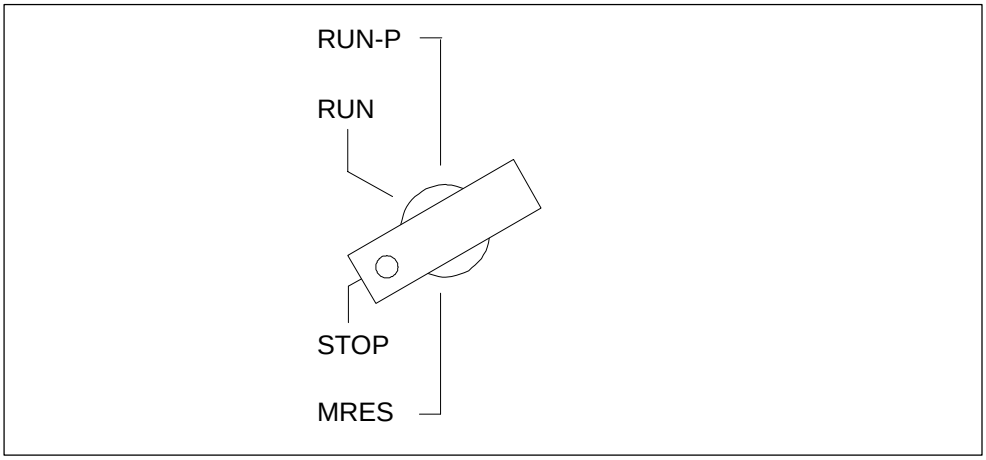


Figure 1-5 Positions of the Mode Selector

Table 1-2 explains the positions of the mode selector. In the event of a fault or if there are startup problems, the CPU will go into or remain in STOP mode irrespective of the position of the mode selector.

Table 1-2 Positions of the Mode Selector

Position	Explanation
RUN-P	If there is no startup problem or error and the CPU can go into RUN, the CPU processes the user program or is idle. It is possible to access the I/O. The key **cannot** be removed in this position. Programs can: • Be read out with the programming device from the CPU (CPU programming device) • Be transferred to the CPU (programming device CPU).
RUN	If there is no startup problem or error and the CPU can go into RUN, the CPU processes the user program or runs in idle. It is possible to access the I/O. The key can be removed in this position to ensure that the mode cannot be changed without authorization. The programming device can read the programs in the CPU (CPU –> PG). **The program in the CPU cannot be changed when the switch is in the RUN position (see STEP 7)! The protection level can be bypassed using a password set in the STEP 7 / Hardware Configuration (STEP 7 V4.02 and above). In other words, if you use this password, the program can also be changed when the switch is in the RUN position.**
STOP	The CPU does not process the user program. The digital signal modules are disabled. The key can be removed in this position to ensure that the operating mode cannot be changed without authorization. Programs can: • Be read out with the programming device from the CPU (CPU programming device) • Be transferred to the CPU (programming device CPU).
MRES (Master Reset)	Momentary-contact position of the key switch for the master reset of the CPU and for cold restart (see the following pages).

Protection Levels

A protection level can be defined in the CPUs of the S7-400 that can be used to protect the programs in the CPU from unauthorized access. You can determine with the protection level which programming device functions a user can execute on the CPU in question without particular authorization (password). You can execute all the programming device functions using a password.

Setting the Protection Levels

You can set the protection levels (1 to 3) for a CPU under STEP 7/Configuring Hardware.

You can remove the protection level set under STEP 7/Configuring Hardware using a manual reset with the mode selector.

You can also set protection levels 1 and 2 using the mode selector. Table 1-3 lists the protection levels of a CPU of the S7-400.

Table 1-3 Protection Levels of a S7-400 CPU

Protection Level	Function	Switch Position
1	• All programming device functions are permitted (default setting).	RUN-P/STOP
2	• It is permissible to load objects from the CPU into programming device. In other words, only read programming device functions are permitted. • Functions for process control, process monitoring and process communication are permitted. • All information functions are permitted.	RUN
3	• Functions for process control, process monitoring and process communication are permitted. • All information functions are permitted.	–

If different protection levels are set with the mode selector and with STEP 7, the higher protection level applies (3 before 2, 2 before 1).

Operating Sequence for Memory Reset

Case A: You want to download a complete, new user program to the CPU.

1. Turn the switch to the STOP position.

   Result: The STOP LED lights up.

2. Turn the switch to the MRES setting and keep it at this setting.

   Result: The STOP LED is dark for a second, light for a second, dark for a second and then remains on.

3. Turn the switch back to the STOP setting, then to the MRES setting again within the next 3 seconds and back to STOP.

   Result: The STOP LED flashes for at least 3 seconds at 2 Hz (memory reset is executed) and then lights up permanently

Case B: When the STOP LED flashes slowly at 0.5 Hz, the CPU is requesting a memory reset (system memory reset request, after a memory card has been removed or inserted, for example).

Turn the switch to MRES and back to the STOP position.

Result: The STOP LED flashes for at least 3 seconds at 2 Hz (reset is being executed) and then remains lit.

You can find the complete description of what happens during a memory reset in the: S7-400, M7-400 Programmable Controllers Installation Manual, Chapter 6.

Cold Restart

The user program is started again following a cold restart. All the data, including the retentive data, are deleted.

Restart

Following a restart, the user program resumes at the position at which it was interrupted.

If the restart after power-on function (automatic restart) is to work, the S7-400 must have a battery backup.

Reboot (Warm Restart)

The user program is started again following a warm restart. The retentive data and the contents of the data blocks are kept.

Operating Sequence at Warm Restart/Reboot/Restart

1. Turn the switch to the STOP position.

   Result: The STOP LED lights up.

2. Turn the switch to the RUN/RUNP setting.

Whether the CPU executes a warm restart/reboot or a restart depends on the parameter assignment for the CPU.

Operating Sequence at Cold Restart

1. Turn the switch to the STOP position.

   Result: The STOP LED lights up.

2. Turn the switch to the MRES setting and keep it at this setting.

   Result: The STOP LED is dark for a second, light for a second, dark for a second and then remains on.

3. Turn the switch to the RUN/RUNP setting.

1.5 Design and Function of Memory Cards

Order Numbers

The order numbers for memory cards are listed in the technical specifications in Chapter 4.

Configuration

The memory card is slightly larger than a credit card and protected by a strong metal casing. It is plugged into a receptacle at the front of the CPU; the end to be inserted is obvious from the design of the memory card.

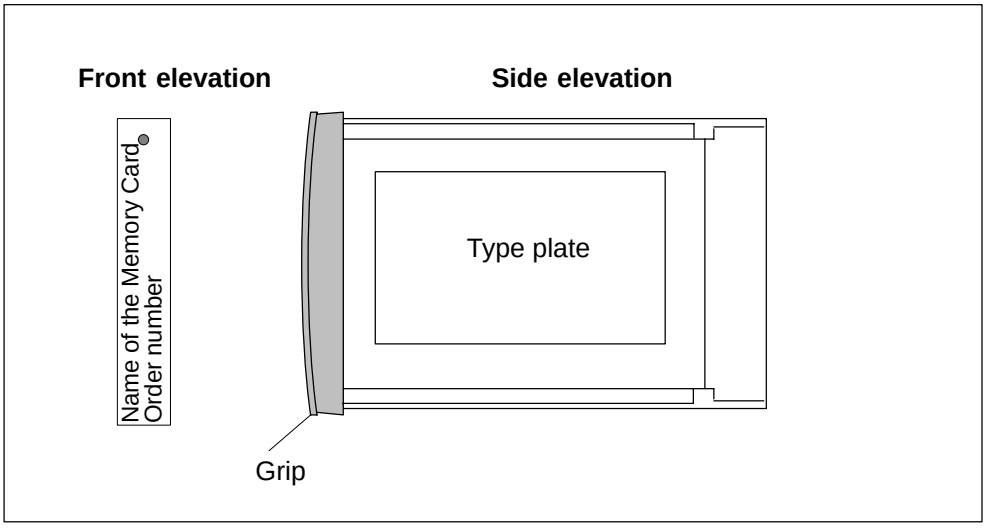


Figure 1-6 Structure of the Memory Card

Function

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. In operation, the load memory contains the complete user program including comments, symbols, special additional information that permits decompiling of the user program, and all the module parameters (see Chapter 2.1).

What the Memory Card Contains

The following data can be stored in the memory card:

- User program, that is, blocks (OBs, FBs, FCs, DBs) and system data
- Parameters that determine the behavior of the CPU
- Parameters that determine the behavior of the I/O modules.
- As of STEP 7 V5.1 the Project in Their Entirety in Suitable Memory Cards.

Types of Memory Cards for the S7-400

Two types of memory card are used in the S7-400:

- RAM cards
- Flash cards (FEPROM cards)

Note

Non-Siemens memory cards cannot be used in the S7-400.

What Type of Memory Card Should You Use?

Whether you use a RAM card or a Flash card depends on how you intend to use the memory card.

Table 1-4 Types of Memory Cards

If you ...	...Then
want to store the data in RAM and you want to modify your program during RUN or RUN-P mode,	use a **RAM card**
want to store your user program permanently on the memory card, even with power removed (without backup or outside the CPU),	use a **Flash card**

RAM Card

you use a RAM card, you must plug this into the CPU to load the user program. The user program is loaded with the help of the programming device (PG).

You can load the entire user program or the individual parts such as FBs, FCs, OBs, DBs, or SDBs into the load memory in STOP mode or in RUN-P mode.

If you remove the RAM card from the CPU, the information stored on it is lost. The RAM card does not have a built-in backup battery.

If the power supply has a functioning backup battery or if an external backup voltage is supplied to the CPU via the “EXT. BATT.” socket, the contents of the RAM card are retained after switching off the power supply provided the RAM card remains plugged into the CPU and the CPU remains in the rack.

Flash Card

If you use a Flash card, there are two ways of loading the user program:

- Set the CPU to STOP with the mode selector, plug the Flash card into the CPU, and load the user program with
  STEP 7 “PLC –> Load User Program to Memory Card”.
- Load the user program into the Flash card in offline mode at the programming device or adapter and then insert the Flash card into the CPU.

You can only load your complete user program with the Flash card. You can load smaller program sections into the integrated load memory on the CPU using the programming device. In the case of larger program changes, you must always reload the Flash card with the complete user program.

The Flash card does not require voltage to store its contents, that is, the information stored on it is retained even when you remove the Flash card from the CPU or if you operate your S7-400 system without backup (without backup battery in the power supply module or “EXT. BATT.” socket of the CPU).

Which Memory Card Capacity to Use

The capacity of the memory card you use depends on the size of the user program and the additional memory requirement resulting from the use of function modules or communications modules. See the manuals of these modules for details of their memory requirements.

To optimally use the working memory (code and data) your CPU, you should expand the load memory of the CPU with a memory card with at least the same capacity as the working memory.

Changing the Memory Card

To change the memory card, follow the steps outlined below:

1. Set the CPU to STOP.
2. Remove the plugged in memory card.

Note

If you remove the memory card, the CPU requests a memory reset by flashing the STOP indicator every three seconds. This sequence cannot be influenced by error OBs.

---

3. Insert a “new” memory card.
4. Perform a memory reset on the CPU.

1.6 Multipoint Interface (MPI)

Connectable Devices

You can, for example, connect the following nodes to the MPI:

- Programming devices (PG/PC)
- Operation and monitoring devices (OPs and TDs)
- Additional SIMATIC S7 programmable controllers

Some connectable devices take a supply of 24 V from the interface. This voltage is available there in non-isolated form.

Programming Device/OP-CPU Communication

A CPU can maintain several simultaneous online connections during communication with programming devices/OPs. By default, one of these connections is for a programming device and one is for an OP/operation and monitoring unit.

For more information about the number of connection resources and the number OPs that can be connected for each CPU, refer to Chapter 4 Technical Specifications.

Communication and Interrupt Response Times

Notice
The interrupt reaction times can be delayed by read and write jobs with a high data volume (approx. 460 byte).

CPU-CPU Communication

There are two types of CPU-CPU communication:

- Data transfer via S7 basic communication
- Data transfer via S7 communication

You can find additional information on this in the “Programming with STEP 7” manual.

Connector

Use only the bus connector with an angular outgoing cable for PROFIBUS DP or a programming device cable for connecting devices to the MPI (see Chapter 7 *in the Installation Manual*).

Multipoint Interface as DP Interface

You can also configure the MPI interface as a DP interface. To do this, you can reconfigure the MPI interface under STEP 7 in SIMATIC Manager. You can use this to set up a DP line with a maximum of 32 slaves.

1.7 PROFIBUS DP Interface

Connectable Devices

You can connect any PROFIBUS DP slave that complies with the standard to the PROFIBUS DP interface.

In this case, the CPU is either a DP master or DP slave connected via the PROFIBUS DP field bus to the passive slave stations or other DP masters.

Some connectable devices take a supply of 24 V from the interface. This voltage is available there in non-isolated form.

Connector

Use only the bus connector for PROFIBUS DP or PROFIBUS cable for connecting devices to the PROFIBUS DP interface (*see* Chapter 7 in the Installation Manual).

1.8 Overview of the Parameters for the S7-400 CPUs

Default Values

All the parameters have default settings at delivery. These defaults, which are suitable for a whole range of standard applications, mean that the S7-400 can be used immediately without the need for further settings.

You can find the CPU-specific default values using “Configuring Hardware” in STEP 7.

Parameter Blocks

The behavior and properties of the CPU are defined using parameters that are stored in system data blocks. The CPUs have a defined default setting. You can change this default setting by modifying the parameters in the hardware configuration.

The following list gives you an overview of the configurable system properties available in the CPUs.

- General properties (e.g. Name of the CPU)
- Startup (e.g. enabling of a restart)
- Clock synchronous interrupts
- Cycle/clock memory (e.g. cycle monitoring time)
- Retentivity (number of memory markers, timers and counters that are maintained)
- Memory (e.g.local data)

  Note: If, for example, you set greater or smaller values than the default values for the process image, the number of diagnostic buffer entries and the maximum number of ALARM-8 blocks (SFB 34 and SFB 35) **and** blocks for S7 communication, the working memory available for the program code and for data blocks will be reduced or increased by this amount.
- Assignment of interrupts (process interrupts, delay interrupts, asynchronous error interrupts) to the priority classes
- Time-of-day interrupts (e.g. start, interval duration, priority)
- Watchdog interrupts (e.g. priority, interval duration)
- Diagnostics/clock (e.g. time synchronization)
- Protection levels

Note

16 memory bytes and 8 counter numbers are set to retentive in the default settings, in other words, they are not deleted when the CPU is restarted.

Parameter Assignment Tool

You can set the individual CPU parameters using “Configuring Hardware” in STEP 7.

Note

If you make changes to the existing settings of the following parameters, the operating system carries out initializations like those during cold restart.

- Size of the process image of the inputs
- Size of the process image of the inputs
- Size of the local data
- Number of diagnostic buffer inputs
- Communication resources

These initializations are:

– Data blocks are initialized with the load values

– Memory bits, times, counts, inputs and outputs are deleted regardless of the retentive settings (0)

– DBs generated via SFC are deleted

– Permanently configured, base communication connections are established

– All the priority classes start from the beginning again

1.9 Multicomputing

Chapter Overview

Section	Description	Page
1.9.1	Peculiarities	1-28
1.9.2	Multicomputing Interrupt	1-29
1.9.3	Configuring and Programming Multicomputing Operation	1-29

What is Multicomputing Operation?

Multicomputing operation is the operation of several (max. 4) multicomputing-capable central processing units at the same time in a central rack (central device) of the S7-400.

The CPUs involved automatically change their modes synchronously. In other words, they start up together and change to STOP mode together. The user program runs on each CPU irrespective of the user programs in the other CPUs. This makes it possible to execute controller tasks in parallel.

When Do You Use Multicomputing?

It is advantageous to use multicomputing in the following cases:

- If your user program is too large for a single CPU and storage space is becoming scarce, distribute your program over several CPUs.
- If a certain part of your system is supposed to be processed quickly, remove the relevant program section from the overall program and have it processed by a separate, “quick” CPU.
- If your system consists of several different parts that can be easily separated from one another and can therefore be controlled relatively independently, let CPU1 process system part 1, CPU 2 system part 2 and so on.

Example

The figure below shows a programmable controller that is working in multicomputing mode. Each CPU can access the modules assigned to it (FM, CP, SM).

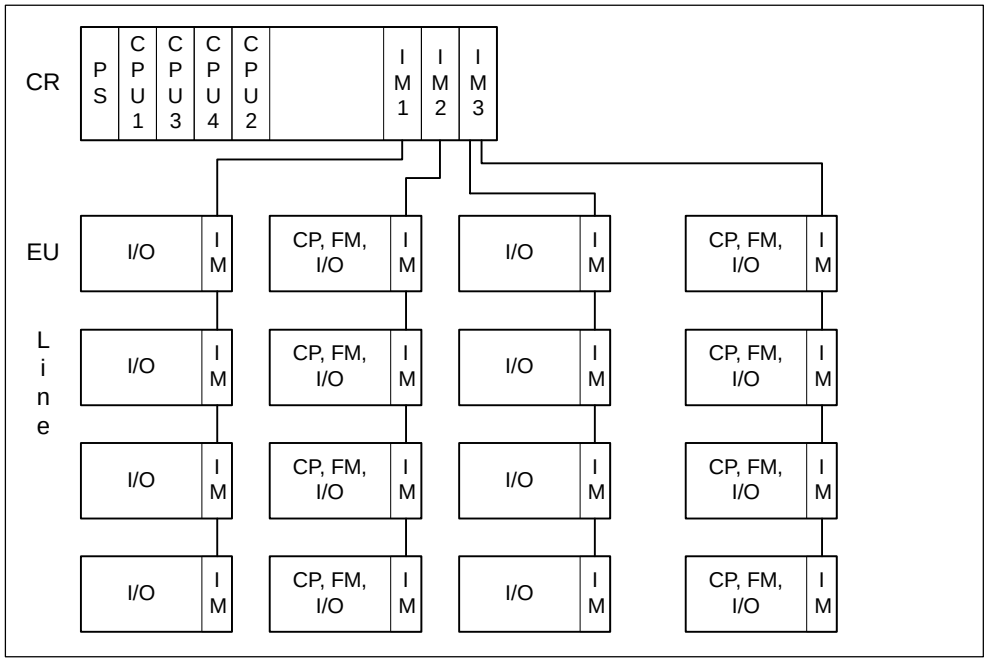


Figure 1-7 Multicomputing Example

The Difference Between Multicomputing Operation and Operation in the Segmented Rack

In the segmented CR2 rack (physically segmented; cannot be done by parameter assignment), only one CPU is allowed per segment. However, this is not multicomputing. The CPUs in the segmented rack each make up an independent subsystem and respond as separate processors. There is no shared logical address area.

Multicomputing operation is not possible in segmented racks (see also the Installation Manual).

1.9.1 Peculiarities

Slot Rules

In multicomputing operation, up to four CPUs can be inserted at the same time in a central controller (CC) in any order.

If you use CPUs that can only handle module start addresses that are divisible by 4 (usually CPUs before 10/98), you must keep to this rule for **all** the configured CPUs when you assign addresses! The rule applies should you also use CPUs that allow the bytewise assignment of module start addresses in single-computing operation.

Bus Connection

The CPUs are connected to one another via the communication bus (K bus). In other words, if configured appropriately, all the CPUs can be reached by the programming device via an MPI interface.

Behavior at Startup and During Operation

At startup, the CPUs involved in multicomputing operation automatically check whether they can synchronize with each other. Synchronization is only possible if:

- All the configured CPUs (but only those) are inserted and not defective.
- Correct configuration data (SDBs) have been created and loaded for all the inserted CPUs.

If one of these prerequisites is not met, the event is entered in the diagnostic buffer with ID 0x49A4. You can find explanations of the event IDs in the reference information for standard and system functions.

When STOP mode is exited, a comparison of the types of startup (COLD RESTART/REBOOT (WARM RESTART/RESTART) is carried out. If their startup type differs, the CPUs do **not** go into RUN mode.

Assignment of Addresses and Interrupts

In multicomputing operation, the individual CPUs can each access the modules that were allocated to them during configuration with STEP 7. The address area of a module is always assigned exclusively to a CPU.

Each interrupt-capable module is assigned to a CPU. Interrupts originating from such a module cannot be received by the other CPUs.

Interrupt Processing

The following applies to interrupt processing:

- Process interrupts and diagnostic interrupts are only sent to one CPU.
- When a module fails or is removed or inserted, the interrupt is processed by the CPU that was assigned to the module at parameter assignment with STEP 7. **Exception:** A module insertion/removal interrupt that starts from a CP reaches all the CPUs even if the CP was assigned to a CPU at configuration with STEP 7.
- In the event of a rack failure, OB 86 is called on each CPU, including CPUs that were not assigned a module in the failed rack.

You can find further information on the OB 86 in the reference information on organization blocks.

Typical I/O Application Specification

The typical I/O application specification of a programmable controller corresponds in multicomputing operation to the typical application specification of the CPU with the most resources. The relevant CPU-specific or DP master-specific typical application specifications cannot be exceeded in the individual CPUs.

1.9.2 Multicomputing Interrupt

Using the multicomputing interrupt (OB 60), you can respond synchronously to an event in multicomputing on the corresponding CPUs. In contrast to the process interrupts triggered by signal modules, the multicomputing interrupt can be output only by CPUs. The multicomputing interrupt is triggered by calling SFC 35 “MP_ALM“.

You will find more information in the *System Software for S7-300/400, System and Standard Functions* manual.

1.9.3 Configuring and Programming Multicomputing Operation

Please refer to the manual *Configuring Hardware and Communication Connections with STEP 7 V5.2* to find out how to configure and program the CPUs and the modules.

1.10 Modifications to the System During Operation

The ability to modify the system during operation using CiR (Configuration in RUN) allows you to make certain changes to the configuration in the RUN mode. Processing is halted for a brief period in order to accomplish this. The upper limit of this time period is set to one second by default but can be changed. During this time, the process inputs retain their most recent value (see the manual, *" Modifications to the System During Operation Using CiR"*

You can download a free copy of this manual from the Internet address:`http://www.siemens.com/automation/service&support`

You can modify the system during operation using CiR in system segments with distributed I/O. This requires a configuration as shown in the following illustration. To simplify the example, only one DP master system and one PA master system are shown. These restrictions do not apply in actual practice.

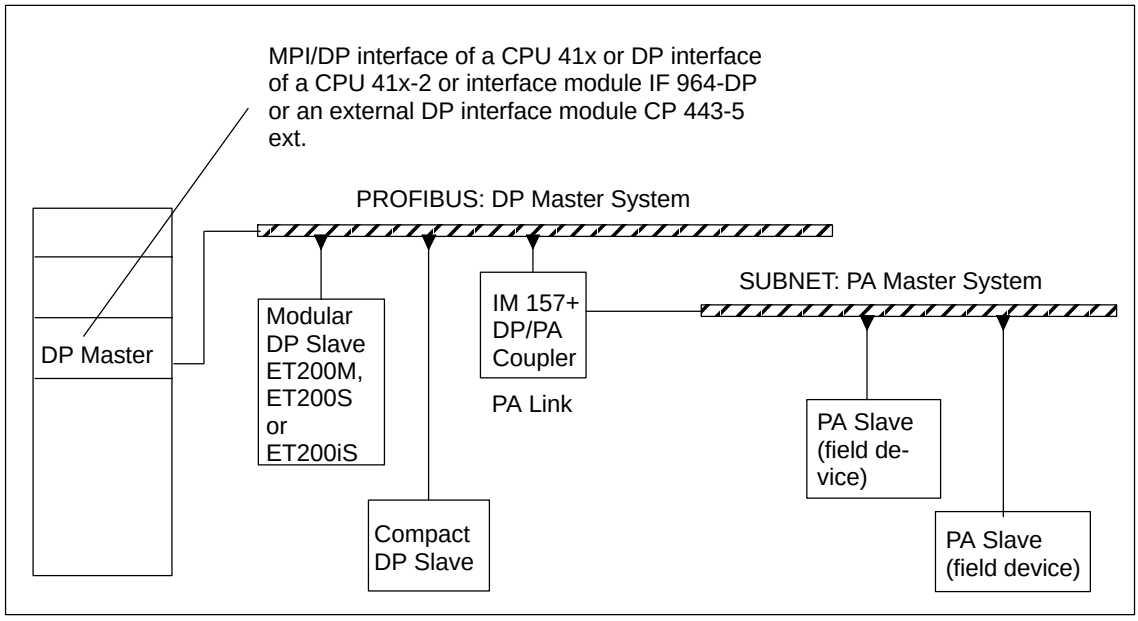


Figure 1-8 Overview: Architecture enabling modification of a system during operation

Hardware Requirements for Modification of a System During Operation

The following hardware requirement must be fulfilled during the commissioning phase in order to be able to subsequently modify the system during operation:

- An S7-400 standard CPU (CPU 412, CPU 414, CPU 416 or CPU 417), firmware V3.1 or later, or an S7-400-H-CPU (CPU 414-4H or CPU 417-4H) in single mode. firmware V3.1 or later.
- If you wish to modify the system during operation on a DP master system with an external DP master (CP 443-5 extended), it must have firmware V5.0 or later.
- If you want to add modules for the ET 200M: Use the IM153-2 version MLFB 6ES7 153-2AA03-0XB0 or later or the IM 153-2FO version MLFB 6ES7 153-2BB00-0XB0 or later. You will also need to install the ET 200M with active bus elements and with enough free space for the planned expansion. You may not install the ET 200M as DPV0 slave (using a GSD file).
- If you wish to add entire stations: be sure to include the required bus connectors, repeaters, etc.
- If you wish to add PA slaves (field devices): use IM157 version 6ES7157-0AA82-0XA00 or later in the corresponding DP/PA Link.
- Rack CR2 cannot be used.
- The cannot use one or more of the following modules within a station where you wish to modify the system during operation using CiR: CP 441-1, CP 441-2, CP 444.
- No multicomputing
- No multimaster configuration
- No use of I-slaves on DP master systems from where you wish to modify the system during operation using CiR.

  If you have configured a CPU 41x as a I-slave on one of your interfaces (MPI/DP, DP or interface module IF 964-DP) and one or more additional DP master systems go out from this CPU (via the other interfaces or via an external DP interface module CP 443-5), then the following applies: you can modify the system during operation using CiR on these additional DP master systems (although you cannot reconfigure the I-slave interface).

Note

You can freely mix components that are cable of system modification during operation and those that are not (except for those listed above). However, you can only make system modifications to CiR-capable components.

Software Requirements for System Modifications During Operation

To be able to change a configuration in RUN mode, the user program must fulfill the following requirement: it must be written in such a way that station failures, module faults or exceeding cycle times does not make the CPU go to STOP.

The following OBs have to be in your CPU:

- Hardware interrupt OBs (OB 40 to OB 47)
- Time error OB (OB 80)
- Diagnostic interrupt OB (OB 82)
- Insert/remove OB (OB 83)
- Program sequence error OB (OB 85)
- Rack failure OB (OB 86)
- I/O access error OB (OB 122)

Permitted system modifications during operation: overview

The following modifications can be made to the system during operation:

- Modules can be added to the modular DP slave ET 200M, if it has not been connected as a DPV0 slave (using a GSD file)
- ET 200M modules can be reconfigured, for example, another interrupt limit can be selected or previously unused channels can be used.
- A previously unused channel in a module or a module for the modular slaves ET 200M, ET 200S, ET 200iS can be used.
- DP slaves can be added to an existing DP master system, but not to I-slaves.
- PA slaves (field devices) can be added to an existing PA master system
- DP/PA couplers can be added behind an IM157
- PA links (including PA master systems) can be added to an existing DP master system
- Modules can be assigned to a process image partition
- Existing modules in ET 200M stations (standard modules and fail-safe signal modules in standard mode) can be reconfigured.
- Reversal of modifications: added modules, DP slaves and PA slaves (field devices) can be removed.

Note

If you wish to add or remove slaves or modules or make changes to an existing assignment to a process image partition, you can only do so on a maximum of four DP master systems.

Any other changes during to the system operation that are not expressly listed above are not allowed and are not included in the this documentation.

1.11 CPU 41x as DP Master/DP Slave

Introduction

This section contains the properties and technical specifications for the CPUs 412-1, 412-2, 414-2, 414-3, 416-2, 416-3 and 417-4 that you will require if you want to use the CPU as a DP master or as a DP slave and configure them for direct communication.

Clarification: Because DP master/DP slave behavior is the same for all CPUs, the CPUs are described as CPU 41x below.

Note

This description applies to CPUs as of V 3.1.

Further References

You can find descriptions of and information on configuration as a whole, the configuration of a PROFIBUS subnetwork and diagnostics in the PROFIBUS subnetwork in the *STEP 7* online help system.

1.11.1 DP Address Areas of the CPUs 41x

Address Areas of the CPUs 41x

Table 1-5 CPUs 41x (MPI/DP Interface as PROFIBUS DP)

Address Area	412-1	412-2	414-2	416-2
MPI interface as PROFIBUS DP, inputs and outputs (bytes) in each case	2048	2048	2048	2048
DP interface as PROFIBUS DP, inputs and outputs (bytes) in each case	–	4096	6144	8192
In the process image, inputs and outputs in each case Can be set up to x bytes	4096	4096	8192	16384

Table 1-6 CPUs 41x (MPI/DP Interface and DP Module as PROFIBUS DP)

Address area	414-3	416-3	417-4
MPI interface as PROFIBUS DP, inputs and outputs (bytes) in each case	2048	2048	2048
DP interface as PROFIBUS DP, inputs and outputs (bytes) in each case	6144	8192	8192
DP module as PROFIBUS DP, inputs and outputs (bytes) in each case	6144	8192	8192
In the process image, inputs and outputs in each case Can be set up to x bytes	8192	16384	16384

DP diagnostic addresses occupy at least one byte for the DP master and each DP slave in the address area. The DP standard diagnosis for each node can be called at these addresses, for example (LADDR parameter of SFC 13). You specify the DP diagnostic addresses during configuration. If you do not specify any DP diagnostic addresses, *STEP 7* assigns the addresses from the highest byte address downwards as DP diagnostic addresses.

In DPV1 mode of the master, the slaves generally have two diagnostic addresses.

1.11.2 CPU 41x as DP Master

Introduction

In this section we describe the features and technical specifications of the CPU if you operate it as a DP master.

You can find the features and technical specifications of the CPUs 41x beginning with Section 4.1.

Requirements

Before commissioning, you must configure the CPU as a DP master. In other words, you must do the following in *STEP 7*

- Configure the CPU as DP master
- Assign a PROFIBUS address
- Select an operating mode (S7-compatible or DPV1)
- Assign a diagnostic address
- Connect DP slaves to the DP master system

Note

Is one of the PROFIBUS DP slaves a CPU 31x or a CPU 41x?

If it is, you will find it in the PROFIBUS DP catalog as a station that has already been configured. Assign this DP slave CPU a slave diagnostic address in the DP master. You must connect the DP master to the DP slave CPU and specify the address areas for the transfer of data to the DP slave CPU.

From EN 50170 to DPV1

The EN 50170 standard for distributed I/O has been further developed. The development results are included in IEC 61158 / IEC 61784-1:2002 Ed1 CP 3/1. In the SIMATIC documentation we refer to this as DPV1. The new version features a few additions and simplifications.

Some SIEMENS automation components already feature DPV1 functions. To be able to use these new features you first have to modify your system a bit. A detailed description of the conversion from EN 50170 to DPV1 is available as FAQ with the title “Changing from EN 50170 to DPV1”, FAQ contribution ID 7027576 at the Customer Support Internet site.

Components Supporting Profibus DPV1 Features

DPV1 Master

- The S7-400 CPUs with integrated DP interface beginning with firmware version 3.0.
- CP 443-5, order number 6GK7 443-5DX03-0XE0, if it to be used with one of these S7-400 CPUs.

DPV1 Slaves

- DP slaves from the hardware catalog of STEP 7 and listed under their family names can be recognized in the information text as DPV1 slaves.
- DP slaves integrated in STEP 7 through GSD files, beginning with GSD Revision 3.

STEP 7

Beginning with STEP 7 V5.1, Service Pack 2.

What are the operating modes for DPV1 components?

- S7 Compatible Mode

  In this mode the components are compatible to EN 50170. However, you cannot fully use the DPV1 features.

- DPV1 Mode

  In this mode you have full access to the DPV1 features. The automation components in the station that do not support DPV1 can continued be used as before.

Compatibility between DPV1 and EN 50170?

You can continue to use all the previous slaves after converting to DPV1. However, your previous slaves do not support the additional functions of DPV1..

You can you use DPV1 slaves even without the conversion to DPV1. The DPV1 slaves then behave like conventional slaves. DPV1 slaves from SIEMENS can be used in the S7-compatible mode. For DPV1 slaves from other manufacturers you need a GSD file to EN50170 earlier than Revision 3.

Switching to DPV1

If you switch to DPV1, then you have to switch the entire station to DPV1 too. You can do this in the STEP 7 hardware configuration (DP mode).

Further Information

You can find descriptions and information on changing from PROFIBUS DP to PROFIBUS DPV1 on the Internet at the following address:

`http://www.siemens.com/automation/service&support`

Under the item number 7027576

Monitor/Modify, Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify.

Note

The applications Programming and Monitor/Modify via the PROFIBUS DP interface extend the DP cycle.

Equidistance

Equidistance is the property of the PROFIBUS DP that guarantees bus cycles of exactly identical length. “Identical length bus cycles” means that the DP master always begins the DP bus cycle after the same time interval. From the view of the slaves, this means that they receive their data from the master at the exact same time intervals.

As of STEP7 V 5.2, you can configure equidistant bus cycles for PROFIBUS subnetworks.

Consistent data

Data that belongs together in terms of its content and a process state written at a specific point in time is known as consistent data.. To maintain consistency, the data should not be changed or updated during processing or transmission.

A detailed description is available in Chapter 1.13.

SYNC/FREEZE

With the SYNC control command, the DP slaves of the selected groups are switched to the Sync mode. In other words, the DP master transfers the current output data and instructs the DP slaves involved to freeze their outputs. With the following output frames, the DP slaves enter the output data in an internal buffer and the state of the outputs remains unchanged.

Following each SYNC control command, the DP slaves of the selected groups apply the output data of their internal buffer to the outputs to the process.

The outputs are only updated cyclically again when you send the UNSYNC control command using SFC 11 “DPSYC_FR”.

With the FREEZE control command, the DP slaves involved are switched to the Freeze mode, in other words the DP master instructs the DP slaves to freeze the current state of the inputs. It then transfers the frozen data to the input area of the CPU..

Following each FREEZE control command, the DP slaves freeze the state of their inputs again.

The DP master only receives the current state of the inputs cyclically again after you have sent the UNFREEZE control command with SFC 11 “DPSYC_FR”.

Power-Up of the DP Master System

Use the following parameters to set power-up monitoring of the DP master:

- Transfer of the Parameters to Modules
- ”Finished” Message by Means of Modules

In other words, the DP slaves must power up and be configured by the CPU (as DP master) in the set time.

PROFIBUS Address of the DP Master

All PROFIBUS addresses are permissible.

1.11.3 Isochrone Updating of the Process Image Partition

With SFC 126 “SYNC_PI“ you can update a process image partition of the inputs synchronous to the clock. A user program linked to a DP cycle can use this SFC to consistently and synchronously update input data located in a process image partition. SFC 126 can be interrupted and can only be called in OBs 61, 62, 63 and 64.

With SFC 127 “SYNC_PO“ you can update a process image partition of the outputs synchronous to the clock. A user program linked to a DP cycle can use this SFC to synchronously update output data located in a process image partition and consistently transmit them to I/O devices. SFC 127 can be interrupted and can only be called in OBs 61, 62, 63 and 64.

To be able to update process image partitions synchronous to the clock, all input or output addresses of a slaves must be assigned to the same process image partition.

To ensure the consistency in a process image partition during each cycle, the following requirements must be fulfilled for each CPUs:

- CPU 412: number of slaves + number of bytes / 100 < 10
- CPU 414: number of slaves + number of bytes / 50 < 20
- CPU 416: number of slaves + number of bytes / 50 < 26
- CPU 417: number of slaves + number of bytes / 50 < 20

SFC 126 and 127 are documented in the corresponding online help and in the manual “System and Standard Functions”.

1.11.4 Diagnostics of the CPU 41x as DP Master

Diagnostics Using LEDs

Table 1-7 explains the meaning of the BUSF LED.
The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 1-7 Meaning of the BUSF LED of the CPU 41x as DP Master

BUSF	Meaning	What to Do
Off	Configuration correct All the configured slaves are addressable	–
Lights	• Bus fault (hardware fault) • DP interface fault • Different transmission rates in multi-DP master operation	• Check the bus cable for a short circuit or interruption. • Evaluate the diagnosis. Reconfigure or correct the configuration.
Flashing	• Station failure • At least one of the assigned slaves is not addressable	• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted. • Wait until the CPU 41x has powered up. If the LED does not stop flashing, check the DP slaves or evaluate the diagnosis of the DP slaves.
Flashes briefly INTF lights up briefly	CiR synchronization running	–

Triggering Detection of the Bus Topology in a DP Master System with the SFC 103 “DP_TOPOL”

The diagnostics repeater is provided to improve the ability to locate disrupted modules or an interruption on the DP cables when failures occur in ongoing operation. This module operates as a slave and can determine the topology of a DP strand and record any faults originating from it.

You can use SFC 103 “DP_TOPOL” to trigger the analysis of the bus topology of a DP master systems by the diagnostics repeater. SFC 103 is documented in the corresponding online help and in the manual “System and Standard Functions”. The diagnostics repeater is documented in the manual “Diagnostics Repeater for PROFIBUS DP”, order number 6ES7 972-0AB00-8BA0.

Reading Out the Diagnosis with STEP 7

Table 1-8 Reading Out the Diagnosis with *STEP 7*

DP Master	Block or Tab in *STEP 7*	Application	Refer To...
CPU 41x	DP slave diagnostics tab	To display the slave diagnosis as plain text at the *STEP 7* user interface	See the section on hardware diagnostics in the *STEP 7* online help system and the *STEP 7* user guide STEP 7-STEP 7
	SFC 13 “DPNRM_DG”	To read out the slave diagnosis (store in the data area of the user program))	For the structure of CPU 41x, see Section 1.11.6; SFC see Reference Manual *System and Standard Functions* For the structure for other slaves, see respective sections
	SFC 59 “RD_REC”	To read out data records of the S7 diagnosis (store in the data area of the user program))	Reference Manual *System and Standard Functions*
	SFC 51 “RDSYSST”	To read out SSL sublists. Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	
	SFB 52 “RDREC”	For DPV1 slaves: To read out data records of the S7 diagnosis (store in the data area of the user program))	
	SFB 54 “RALRM”	For DPV1 slaves: To read out interrupt information within the associated interrupt OB	
	SFC 103 ”DP_TOPOL”	Triggers detection of the bus topology of a DP master system with diagnostic repeaters installed there.	

Evaluating the Diagnosis in the User Program

The following figure shows you how to evaluate the diagnosis in the user program.

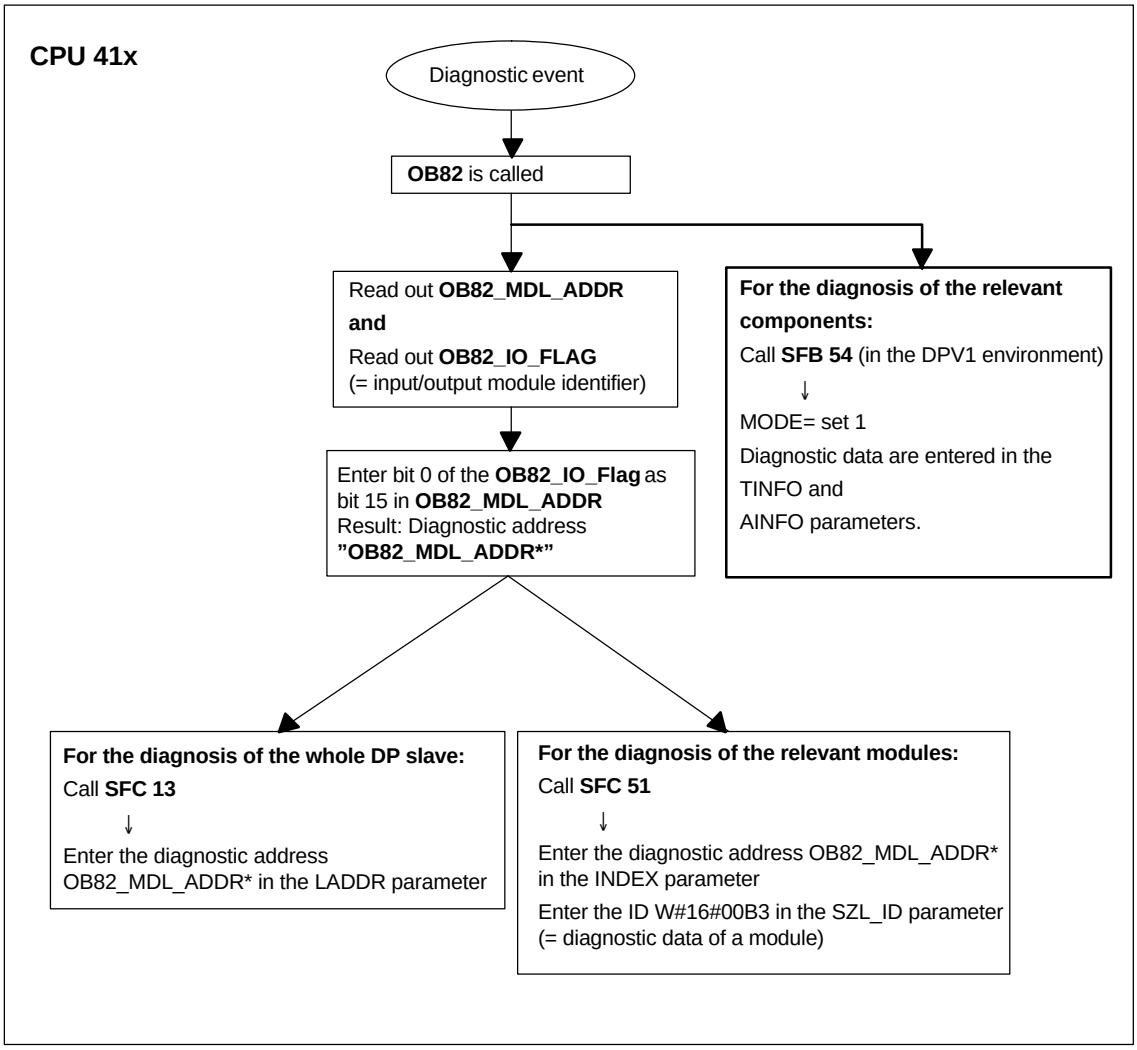


Figure 1-9 Diagnostics with CPU 41x

Diagnostic Addresses in Connection with DP Slave Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

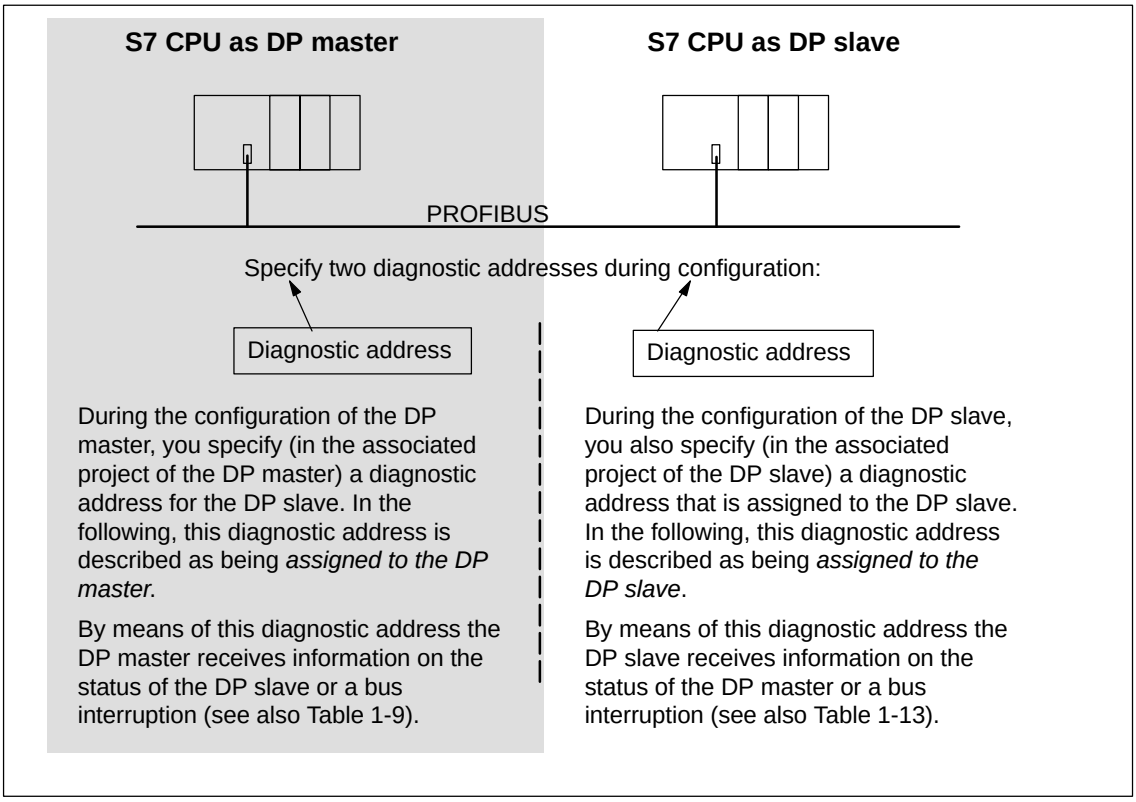


Figure 1-10 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 1-9 shows you how the CPU 41x as DP master detects any changes in the operating mode of a CPU as DP slave or interruptions in data transfer.

Table 1-9 Event Detection of the CPUs 41x as DP Master

Event	What Happens in the DP Master
Bus interruption (short circuit, connector removed)	• OB 86 called with the message *Station failure* (incoming event; diagnostic address of the DP slave that is assigned to the DP master) • In the case of I/O access: OB 122 called (I/O access error)
DP slave: RUN → STOP	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=1)
DP slave: STOP → RUN	• OB 82 is called with the message *Module OK.* (outgoing event; diagnostic address of the DP slave that is assigned to the DP master; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table shows you how, for example, you can evaluate RUN-STOP transitions of the DP slave in the DP master (see also Table 1-9).

In the DP Master		In the DP Slave (CPU 41x)
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**		Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=not relevant
The CPU calls OB 82 with the following information, amongst other things: • OB 82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module malfunction Tip: This information is also in the diagnostic buffer of the CPU You should also program the SFC 13 “DPNRM_DG” in the user program to read out the DP slave diagnostic data. We recommend you use SFB 54 in the DPV1 environment. It outputs the interrupt information in its entirety.	←	CPU: RUN → STOP CPU generates a DP slave diagnostic frame .

1.11.5 CPU 41x as DP Slave

Introduction

In this section we describe the features and technical specifications of the CPU if you operate it as a DP slave.

You can find the features and technical specifications of the CPUs 41x as of Section 4.1.

Requirements

1. Only one DP interface of a CPU can be configured as a DP slave.
2. Is the MPI/DP interface to be a DP interface? If so, you must configure the interface as a DP interface.

   Before commissioning you must configure the CPU as a DP slave. In other words, you must do the following in *STEP 7*

   – Activate the CPU as a DP slave

   – Assign a PROFIBUS address

   – Assign a slave diagnostic address

   – Define the address areas for data transfer to the DP master

DDB (GSD) Files

You need a DDB file to configure the CPU as a DP slave in a third-party system.

You can download the GSD file free of charge from the Internet at http://www.ad.siemens.de/csi_e/gsd.

You can also download the GSD file from the mailbox of the Interface Center in Fürth on +49 (911) 737972.

Configuration and Parameter Assignment Frame

When you configure and assign parameters to CPU 41x, you are supported by *STEP 7*. If you require a description of the configuration and parameter assignment frame to carry out a check with a bus monitor, for example, you will find it on the Internet at http://www.ad.siemens.de/simatic-cs under the ID 1452338

Monitor/Modify, Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify. To do this, you must enable these functions when you configure the CPU as DP slave in *STEP 7*.

Note

The use of Programming or Monitor and Modify via the PROFIBUS DP interface extends the DP cycle.

Data Transfer Via an Intermediate Memory

As a DP slave the CPU 41x makes an intermediate memory available to PROFIBUS DP. Data transfer between the CPU as DP slave and the DP master always takes place via this intermediate memory. You can configure up to 32 address areas for this.

In other words, the DP master writes its data in these address areas of the intermediate memory and the CPU reads the data in the user program and vice versa.

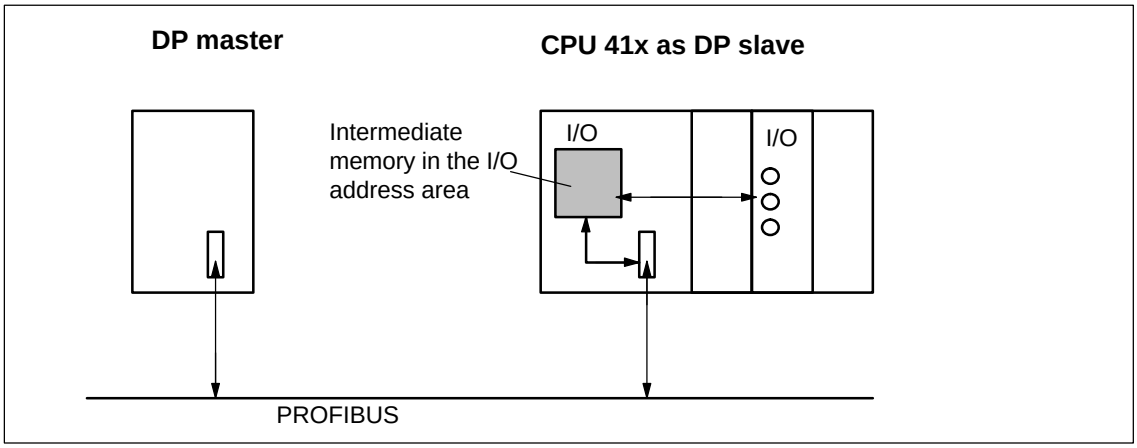


Figure 1-11 Intermediate Memory in the CPU 41x as DP Slave

Address Areas of the Intermediate Memory

Configure in *STEP 7* the input and output address areas:

- You can configure up to 32 input and output address areas.
- Each of these address areas can be up to 32 bytes in size
- You can configure a maximum of 244 bytes of inputs and 244 bytes of outputs in total

An example for the configuration of the address assignments of the intermediate memory is provided in the table below. You will also find this in the online help for STEP 7 configuration.

Table 1-10 Configuration Example for the Address Areas of the Intermediate Memory

	Type	Master Address	Type	Slave Address	Length	Unit	Consistency
1	e	222	A	310	2	Byte	Unit
2	A	0	e	13	10	Word	Total length
:							
32							
	Address areas in the DP master CPU		Address areas in the DP slave CPU		These parameters of the address areas must be the same for the DP master and DP slave		

Rules

You must adhere to the following rules when working with the intermediate memory:

- Assignment of the address areas:
  - Input data of the DP slave are **always** output data of the DP master
  - Output data of the DP slave are **always** input data of the DP master
- You can assign the addresses as you choose. You access the data in the user program with load/transfer commands or with SFCs 14 and 15. You can also specify addresses from the process image input and output table (see also section 1.11.1).

Note

You assign addresses for the intermediate memory from the DP address area of the CPU 41x.

You must not reassign the addresses you have already assigned to the intermediate memory to the I/O modules on the CPU 41x.

- The lowest address in each address area is the start address of that address area.
- The length, unit and consistency of address areas for the DP master and DP slave that belong together must be the same.

S5 DP Master

If you use an IM 308 C as a DP master and the CPU 41x as a DP slave, the following applies to the exchange of consistent data:

You must program FB 192 in the IM 308-C so that consistent data can be transferred between the DP master and DP slave. The data of the CPU 41x are only output or displayed contiguously in a block with FB 192.

S5-95 as DP Master

If you use an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 41x as DP slave.

Sample Program

The small sample program below illustrates data transfer between the DP master and DP slave. This example contains the addresses from Table 1-10.

In the DP Slave CPU	In the DP Master CPU

`L 2 Preprocess data`
`T MB 6 in the DP slave`
`L EB 0`
`T MB 7`
 	
`L MW 6 Transfer data to`
`T PQW 310 the DP master`	

	`L PIB 222 Continue to`
	`T MB 50 process received`
	`L PIB 223 data in the DP`
	`L B#16#3 master`
	`+ I`
	`T MB 51`
	
	`L 10 Preprocess data`
	`+ 3 in the DP master`
	`T MB 60`
	
	`CALL SFC 15 Send data to the`
	`LADDR:= W#16#0 DP slave`
	`RECORD:= P#M60.0 Byte20`
	`RET_VAL:= MW 22`

`CALL SFC 14 Receive data`
`LADDR:=W#16#D from the DP`
`RET_VAL:=MW 20 master`
`RECORD:=P#M30.0 Byte20`
 	
`L MB 30 Continue to`
`L MB 7 process received`
`+ I data`
`T MW 100`	

Data Transfer in STOP Mode

The DP slave CPU goes into STOP mode: The data in the intermediate memory of the CPU are overwritten with “0”. In other words, the DP master reads “0”.

The DP master goes into STOP mode: The current data in the intermediate memory of the CPU are retained and can continue to be read by the CPU.

PROFIBUS Address

You cannot set 126 as PROFIBUS address for the CPU 41x as DP slave.

1.11.6 Diagnostics of the CPU 41x as DP Slave

Diagnostics using LEDs – CPU 41x

Table 1-11 explains the meaning of the BUSF LEDs.
The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 1-11 Meaning of the BUSF LEDs of the CPU 41x as DP Slave

BUSF	Meaning	What to Do
Off	Configuration correct	–
Flashing	The CPU 41x is incorrectly configured. There is no data interchange between the DP master and the CPU 41x. Causes: • The response monitoring time has expired. • Bus communication via PROFIBUS DP has been interrupted. • The PROFIBUS address is incorrect.	• Check the CPU 41x. • Check to make sure that the bus connector is properly inserted. • Check whether the bus cable to the DP master has been interrupted. • Check the configuration and parameter assignment.
On	• Bus short circuit	• Check the bus setup.

Triggering Detection of the Bus Topology in a DP Master System with the SFC 103 “DP_TOPOL”

The diagnostics repeater is provided to improve the ability to locate disrupted modules or an interruption on the DP cables when failures occur in ongoing operation. This module operates as a slave and can determine the topology of a DP strand and record any faults originating from it.

You can use SFC 103 “DP_TOPOL” to trigger the analysis of the bus topology of a DP master systems by the diagnostics repeater. SFC 103 is documented in the corresponding online help and in the manual “System and Standard Functions”. The diagnostics repeater is documented in the manual “Diagnostics Repeater for PROFIBUS DP”, order number 6ES7-972-0AB00-8BA0.

Diagnostics with *STEP 5* or *STEP 7* Slave Diagnostics

The slave diagnosis complies with the EN 50170, Volume 2, PROFIBUS standard. Depending on the DP master, it can be read out with *STEP 5* or *STEP 7* for all DP slaves that comply with the standard.

The display and structure of the slave diagnosis is described in the following sections.

S7 Diagnosis

An S7 diagnosis can be requested for all diagnostics-capable modules in the SIMATIC S7/M7 range of modules in the user program. You can find out which modules have diagnostic capability in the module information or in the catalog. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current status of a module. Data record 1 also contains module-specific diagnostic data.

You will find the structure of the diagnostic data described in the *Standard and System Functions* Reference Manual.

Reading Out the Diagnosis

Table 1-12 Reading Out the Diagnostic Data with *STEP 5* and *STEP 7* in the Master System

Automation System with DP Master	Block or Tab in *STEP 7*	Application	Refer To...
SIMATIC S7/M7	DP slave diagnostics tab	To display the slave diagnosis as plain text at the *STEP 7* user interface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *STEP 7* user guide STEP 7
	SFC 13 “DP NRM_DG”	To read out the slave diagnosis (store in the data area of the user program))	SFC see Reference Manual *System and Standard Functions*
	SFC 51 “RDSYSST”	To read out SSL sublists Call SFC 51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	See the *System and Standard Functions* Reference Manual
	SFB 54 “RDREC”	Applies to the DPV1 environment: To read out interrupt information within the associated interrupt OB	
	FB 125/FC 125	To evaluate slave diagnosis	The Internet page http://www.ad.siemens.de/simatic-cs ID 387 257

Table 1-12 Reading Out the Diagnostic Data with *STEP 5* and *STEP 7* in the Master System, Fortsetzung

Automation System with DP Master	Block or Tab in *STEP 7*	Application	Refer To...
SIMATIC S5 with IM 308-C as DP master	FB 192 “IM308C”	To read out the slave diagnosis (store in the data area of the user program)	FBs see the *ET 200 Distributed I/O System manual*
SIMATIC S5 with S5-95U programmable controller as DP master	SFB 230 “S_DIAG”		

Example of Reading Out the Slave Diagnosis with FB 192 “IM 308C”

Here you will find an example of how to use FB 192 to read out the slave diagnosis for a DP slave in the *STEP 5* user program.

Assumptions

The following assumptions apply to this *STEP 5* user program:

- The IM 308-C is assigned pages 0 to 15 (number 0 of the IM 308-C) as the DP master.
- The DP slave has the PROFIBUS address 3.
- The slave diagnosis is to be stored in DB 20. However, you can also use any other data block for this.
- The slave diagnosis consists of 26 bytes.

STEP 5 User Program

```
STL                                 Explanation
        :A      DB 30
        :JU     FB 192
Name    :IM308C
DPAD    :       KH F800             Default address area of the IM 308-C
IMST    :       KY 0, 3             IM no. = 0, PROFIBUS address of DP slave = 3
FCT     :       KC SD               Function: Read slave diagnosis
GCGR    :       KM 0                Not evaluated
TYP     :       KY 0, 20            S5 data area: DB 20
STAD    :       KF +1               Diagnostic data from data word 1
LENG    :       KF 26               Length of diagnosis = 26 bytes
ERR     :       DW 0                Error code stored in DW 0 of DB 30
```

Diagnostic Addresses in Connection with DP Master Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Ensure during configuration that DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

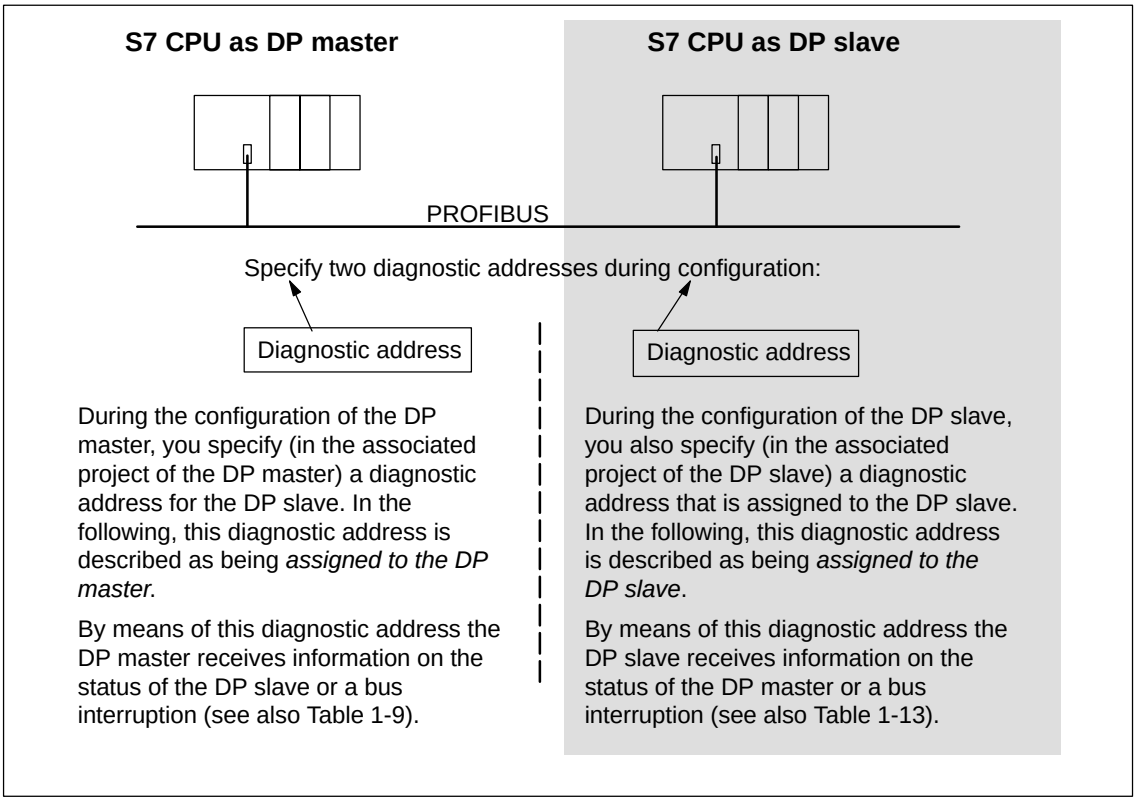


Figure 1-12 Diagnostic Addresses for the DP Master and DP Slave

Event Detection

Table 1-13 shows you how the CPU 41x as DP slave detects any operating mode changes or interruptions in data transfer.

Table 1-13 Event Detection of the CPUs 41x as DP Slave

Event	What Happens in the DP Slave
Bus interruption (short circuit, connector removed)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the DP slave that is assigned to the DP slave) • In the case of I/O access: OB 122 called (I/O access error)
DP master: RUN → STOP	• OB 82 is called with the message *Faulty module* (incoming event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=1)
DP master: STOP → RUN	• OB 82 is called with the message *Module OK*. (outgoing event; diagnostic address of the DP slave that is assigned to the DP slave; Variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table 1-14 shows you, for example, how you can evaluate RUN-STOP transitions of the DP master in the DP slave (see also Table 1-13).

Table 1-14 Evaluation of RUN-STOP Transitions in the DP Master/DP Slave

In the DP Master	In the DP Slave
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic addresses: (example) Slave diagnostic address=**422** Master diagnostic address=not relevant
CPU: RUN → STOP →	The CPU calls OB 82 with the following information, amongst other things: • OB 82_MDL_ADDR:=**422** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module malfunction Tip: This information is also in the diagnostic buffer of the CPU

Structure of the Slave Diagnosis

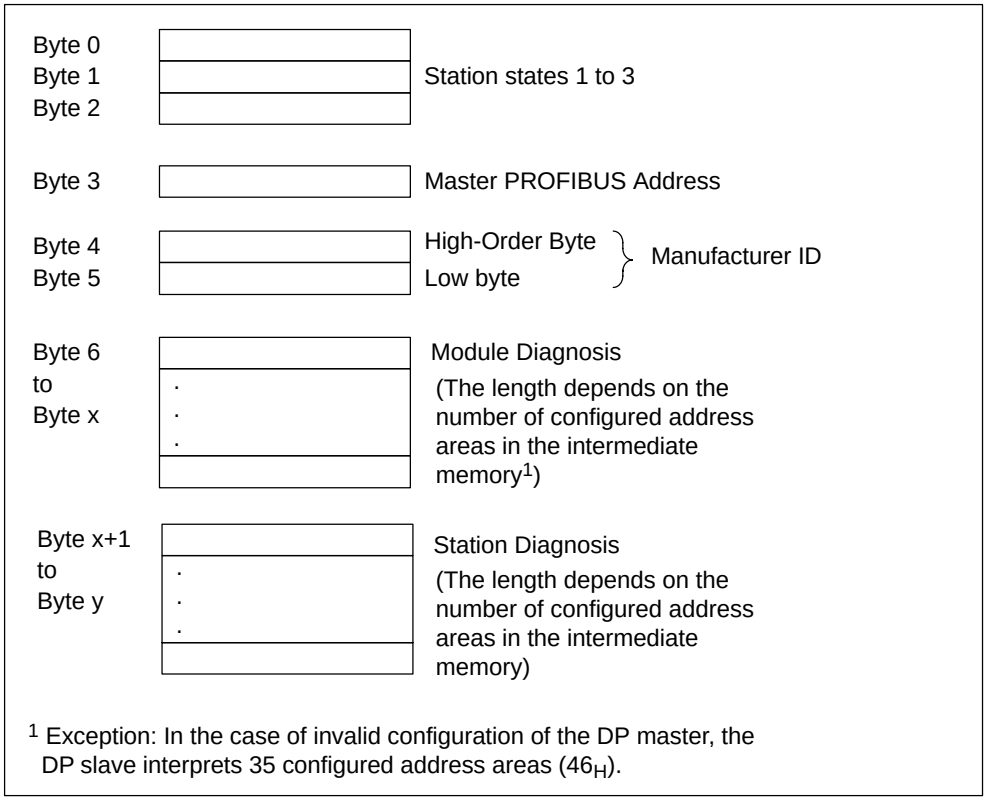


Figure 1-13 Structure of the Slave Diagnosis

1.11.7 CPU 41x as DP slave: Station States 1 to 3

Station states 1 to 3

Station status 1 to 3 provides an overview of the status of a DP slave.

Table 1-15 Structure of the Station Status 1 (Byte 0)

Bit	Meaning	What to Do
0	1: The DP slave **cannot** be addressed by the DP master.	• Correct DP address set on the DP slave? • Bus connector connected? • Voltage on DP slave? • RS 485 repeater set correctly? • Execute reset on the DP slave
1	1: The DP slave is not yet ready for data transfer.	• Wait while the DP slave powers up.
2	1: The configuration data sent by the DP master to the DP slave does not correspond to the actual configuration of the DP slave.	• Correct station type or correct configuration of the DP slave entered in the software?
3	1: Diagnostic interrupt, triggered by RUN-STOP transition of the CPU 0: Diagnostic interrupt, triggered by STOP-RUN transition of the CPU	• You can read out the diagnosis.
4	1:Function is not supported, e.g. changing the DP address via software	• Check the configuration.
5	0: The bit is always “0”.	–
6	1: The DP slave type does not correspond to the software configuration.	• Correct station type entered in the software? (Parameter assignment error)
7	1: Parameters have been assigned to the DP slave by a different DP master to the one that currently has access to the DP slave.	• Bit is always at 1, when you are accessing the DP slave using the programming device or another DP master, for example. The DP address of the parameter assignment master is in the “master PROFIBUS address” diagnostic byte.

Table 1-16 Structure of Station Status 2 (Byte 1)

Bit	Meaning
0	1: The DP slave must be assigned new parameters and reconfigured.
1	1: A diagnostic message has been issued. The DP slave cannot continue until the problem has been corrected (static diagnostic message).
2	1: The bit is always set to “1” if the DP slave with this DP address is present.
3	1: Response monitoring is enabled for this DP slave.
4	0: The bit is always at “0”.
5	0: The bit is always at “0”.
6	0: The bit is always at “0”.
7	1: The DP slave is disabled – that is, it has been removed from cyclic processing.

Table 1-17 Structure of Station Status 3 (Byte 2)

Bit	Meaning
0 to 6	0: The bits are always at “0”.
7	1: • There are more diagnostic messages than the DP slave can store. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

Master PROFIBUS Address

The master PROFIBUS address diagnostic byte contains the DP address of the DP master that:

- Assigns parameters for the DP slave and
- Has read and write access to the DP slave

Table 1-18 Structure of the Master PROFIBUS Address (Byte 3)

Bit	Meaning
0 to 7	DP address of the DP master that configured the DP slave and has read and write access to the DP slave.
	FF_H: DP slave has not been configured by any DP master.

Manufacturer ID

The manufacturer ID contains a code that describes the type of the DP slave.

Table 1-19 Structure of the Manufacturer ID (Bytes 4, 5)

Byte 4	Byte 5	Manufacturer ID for CPU
80_H	$C5_H$	412-1
80_H	$C6_H$	412-2
80_H	$C7_H$	414-2
80_H	$C8_H$	414-3
80_H	CA_H	416-2
80_H	CB_H	416-3
80_H	CC_H	417-4

Module Diagnosis

The module diagnosis tells you for which of the configured address areas of the intermediate memory an entry has been made.

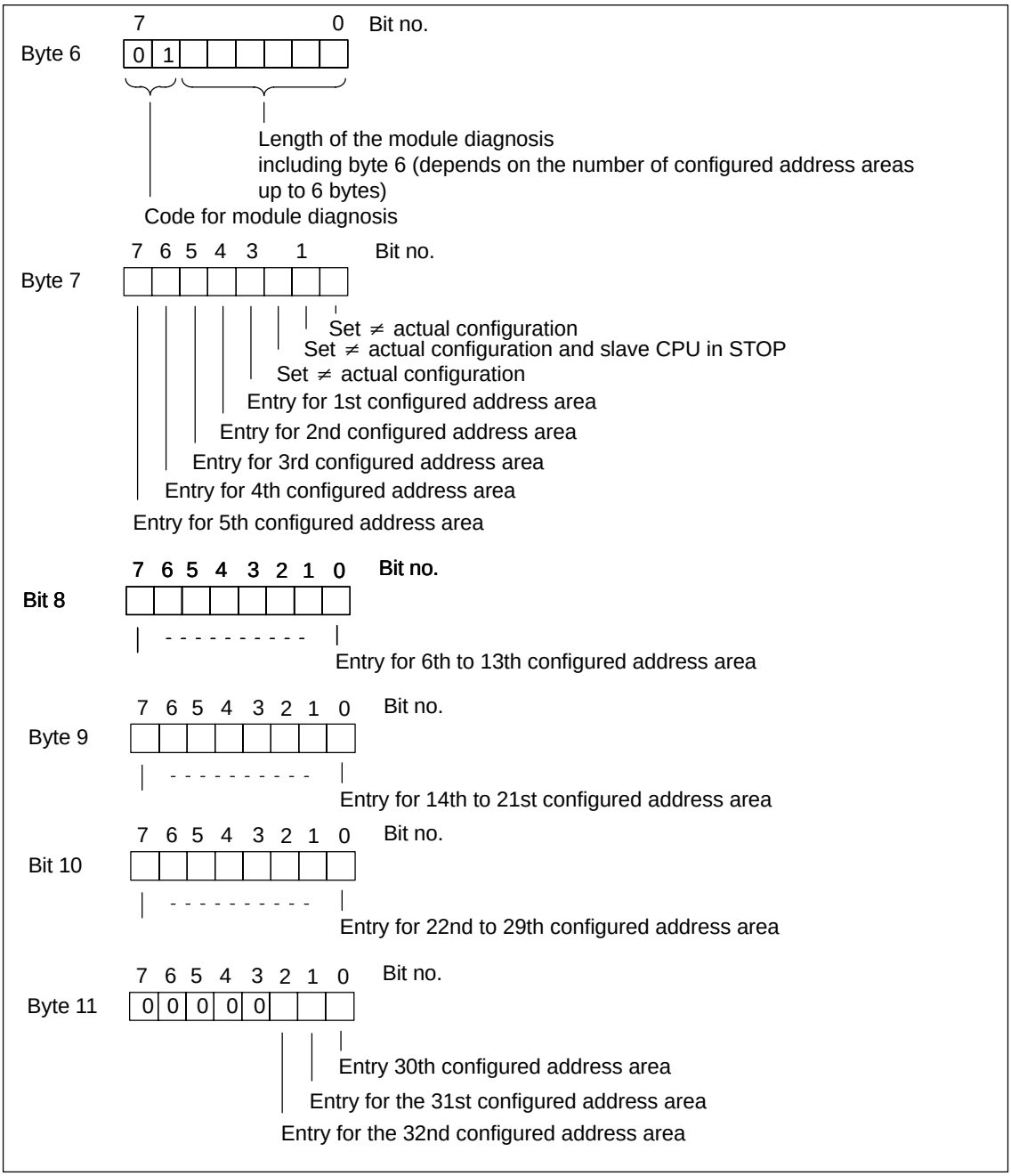


Figure 1-14 Structure of the Module Diagnosis of the CPU 41x

Station Diagnosis

The station diagnosis provides detailed information on a DP slave. The station diagnosis starts as of byte x and can include up to 20 bytes.

The figure below illustrates the structure and contents of the bytes for a configured address area of the intermediate memory.

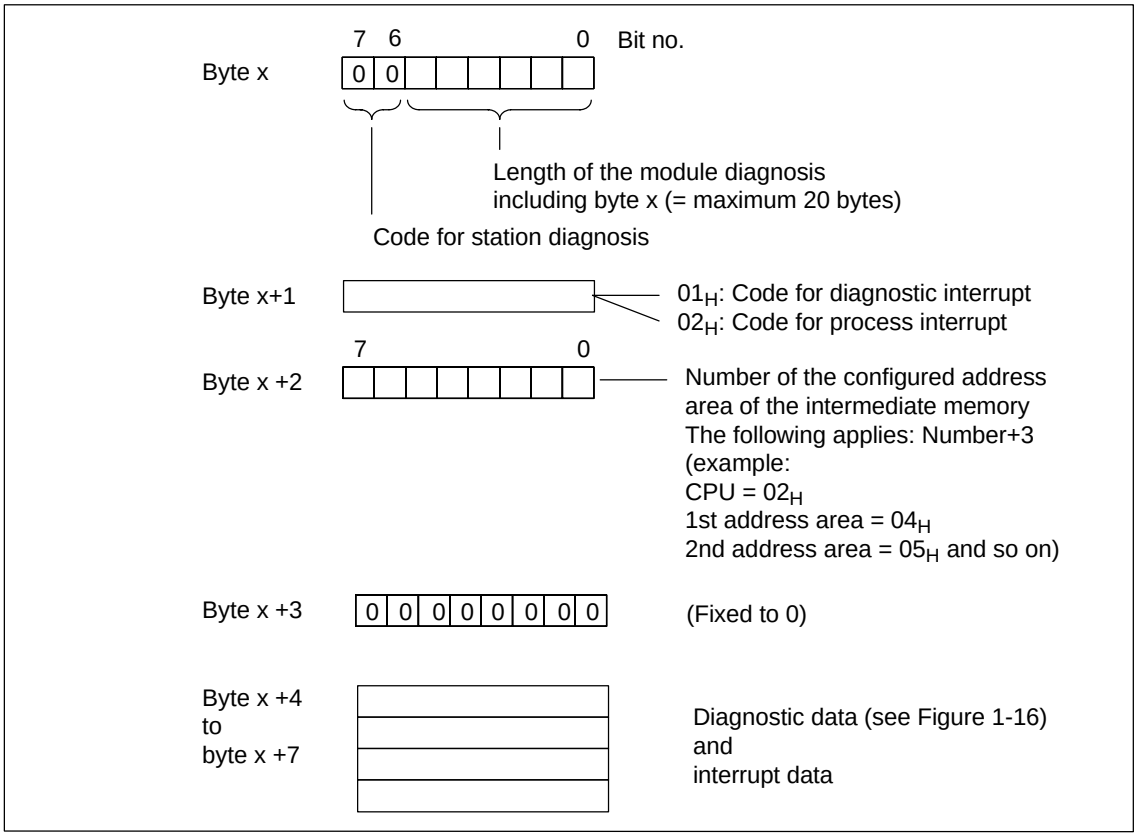


Figure 1-15 Structure of the Station Diagnosis

As of byte x +4

The meaning of the bytes as of byte x+4 depends on byte x +1 (see Figure 1-15).

In Byte x +1, the Code Stands for:	
Diagnostic Interrupt (01_H)	**Process Interrupt (02_H)**
The diagnostic data contain the 16 byte status information of the CPU. Figure 1-16 shows you the assignment of the first 4 bytes of the diagnostic data. The following 12 bytes are always 0.	You can program 4 bytes of interrupt information any way you wish for the process interrupt. You transfer these 4 bytes to the DP master in *STEP 7* using SFC 7 “DP_PRAL”.

Bytes x+4 to x+7 for Diagnostic Interrupts

Figure 1-16 illustrates the structure and contents of bytes x +4 to x +7 for the diagnostic interrupt. The contents of these bytes correspond to the contents of data record 0 of the diagnosis in *STEP 7* (in this case not all the bits are assigned).

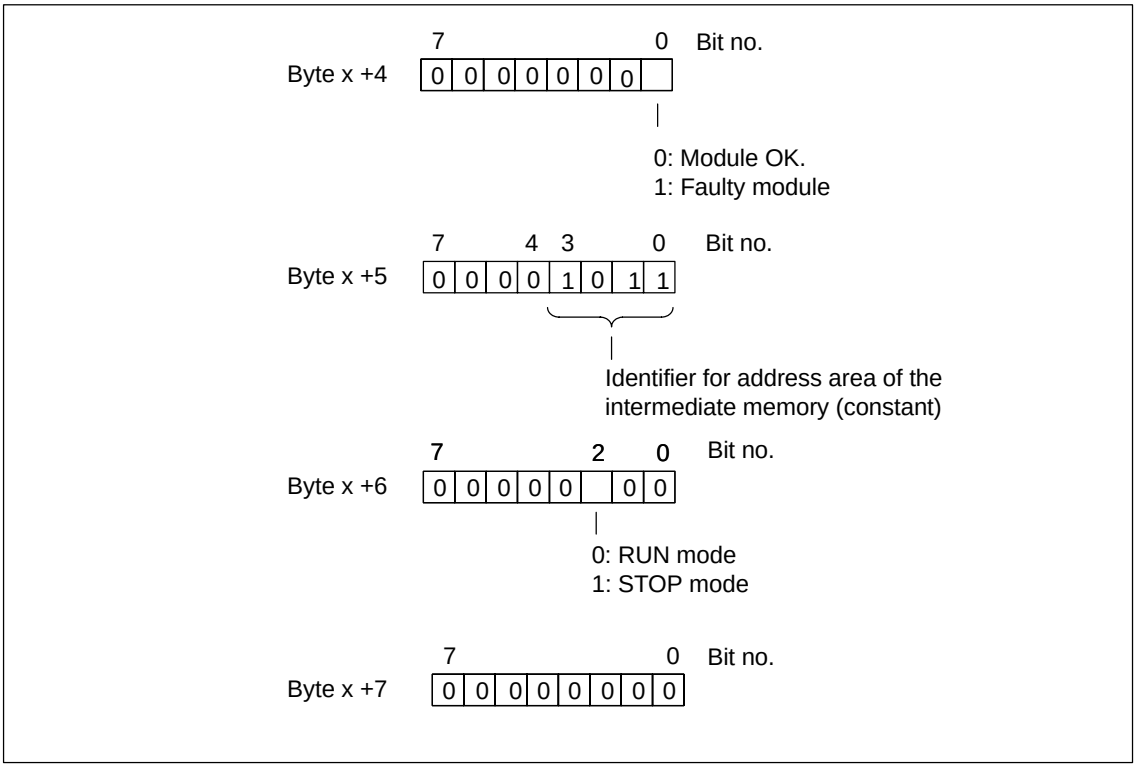


Figure 1-16 Bytes +4 to +7 for Diagnostic and Process Interrupts

Interrupts with the S7/M7 DP Master

In the CPU 41x as a DP slave you can trigger a process interrupt in the DP master from the user program. You can trigger an OB 40 in the user program of the DP master by calling SFC 7 “DP_PRAL”. Using SFC 7 you can forward interrupt information in a double word to the DP master, which you can evaluate in OB 40 in the OB40_POINT_ADDR variable. You can program the interrupt information as you choose. You will find a detailed description of SFC 7 “DP_PRAL” in the *System Software for S7-300/400, System and Standard Functions* Reference Manual.

Interrupts with another DP Master

If you are running the CPU 41x with another DP master, these interrupts are reflected in the station diagnosis of the CPU 41x. You have to process the relevant diagnostic events in the DP master’s user program.

Note

Note the following in order to be able to evaluate diagnostic interrupts and process interrupts by means of the station diagnosis when using a different DP master:

- The DP master should be able to store the diagnostic messages; in other words, the diagnostic messages should be stored in a ring buffer in the DP master. There are more diagnostic messages than the DP master can store, only the last diagnostic message received would be available for evaluation, for example.
- You must query the relevant bits in the station diagnosis at regular intervals in your user program. You must also take the PROFIBUS DP bus cycle time into consideration so that you can query the bits at least once synchronously with the bus cycle time, for example.
- You cannot use process interrupts in the station diagnosis with an IM 308-C as the DP master, because only incoming – and not outgoing – interrupts are reported.

1.12 Direct Communication

You can configure direct communication for PROFIBUS nodes as of *STEP 7* V 5.x. The CPU 41x can participate in direct communication as the sender or recipient.

“Direct Communication” represents a special type of communication relationship between PROFIBUS DP nodes.

1.12.1 Principle of Direct Data

Direct communication is characterized by the fact that PROFIBUS DP nodes “listen in” to find out which data a DP slave is sending back to its DP master. By means of this mechanism the “eavesdropper” (recipient) can access changes to the input data of remote DP slaves directly.

During configuration in *STEP 7*, you specify by means of the relevant I/O input addresses the address area of the recipient to which the required data of the sender are to be read.

A CPU 41x can be:

Sender	as a DP slave
Recipient	as a DP slave or a DP master or as a CPU that is not integrated in a master system (see Figure 1-17).

Example

Figure 1-17 uses an example to illustrate which direct communication “relationships” you can configure. All the DP masters and DP slaves in the figure are CPUs 41x. Note that other DP slaves (ET 200M, ET 200X, ET 200S) can only be senders.

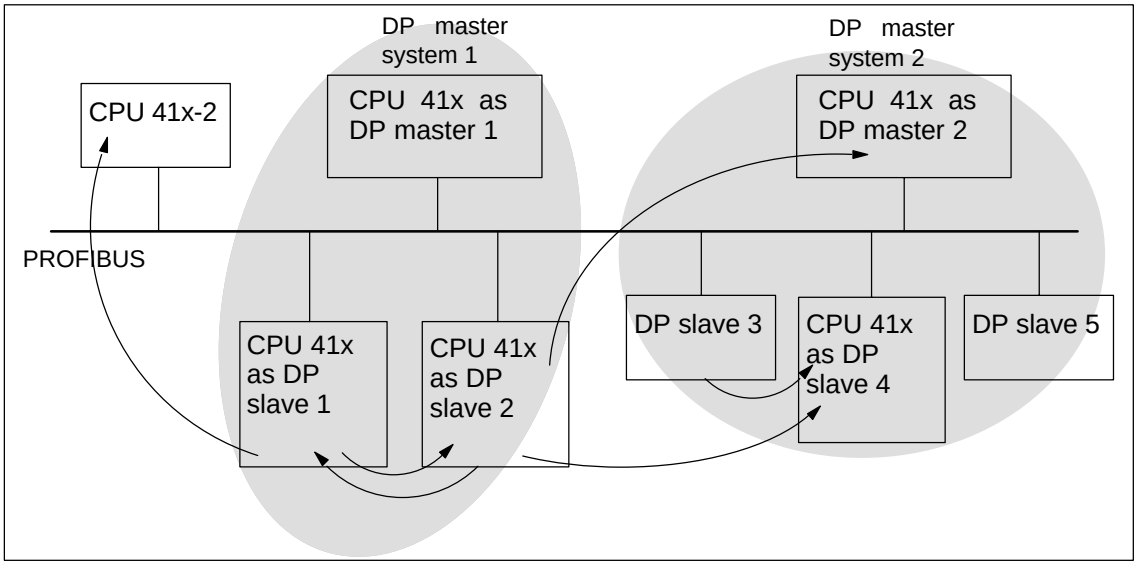


Figure 1-17 Direct Communication with CPUs 41x

1.12.2 Diagnostics in Direct Communication

Diagnostic Addresses

In direct communication you assign a diagnostic address in the recipient:

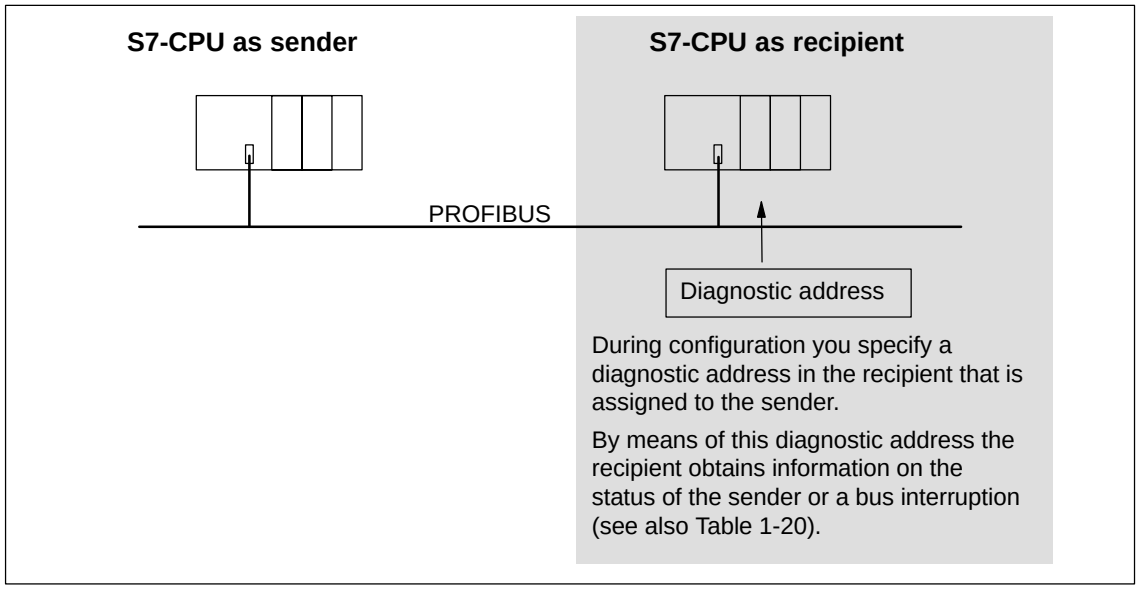


Figure 1-18 Diagnostic Address for the Recipient During Direct Communication

Event Detection

Table 1-20 shows you how the CPU 41x as recipient detects interruptions in data transfer.

Table 1-20 Event Detection of the CPUs 41x as Recipient During Direct Communication

Event	What Happens in the Recipient
Bus interruption (short circuit, connector removed)	• OB 86 is called with the message *Station failure* (incoming event; diagnostic address of the recipient assigned to the sender) • In the case of I/O access: OB 122 called (I/O access error)

Evaluation in the User Program

The following table 1-21 shows you, for example, how you can evaluate a sender station failure in the recipient (see also Table 1-20).

Table 1-21 Evaluation of the Station Failure in the Sender During Direct Communication

In the Sender	In the Recipient
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic address: (example) Diagnostic address=**444**
Station failure →	The CPU calls OB 86 with the following information, amongst other things: • OB 86_MDL_ADDR:=**444** • OB86_EV_CLASS:=B#16#38 (incoming event) • OB86_FLT_ID:=B#16#C4 (failure of a DP station) Tip: This information is also in the diagnostic buffer of the CPU

1.13 Consistent Data

Data that belongs together in terms of its content and a process state written at a specific point in time is known as consistent data. To maintain consistency, the data should not be changed or updated during processing or transmission.

Example

To ensure that the CPU has a consistent image of the process signals for the duration of cyclic program scanning, the process signals are read from the process image inputs prior to program scanning and written to the process image outputs after the program scanning. Subsequently, during program scanning when the address area “inputs” (I) and “outputs” (O) are addressed, the user program addresses the internal memory area of the CPU on which the image of the inputs and outputs is located instead of directly accessing the signal modules.

SFC 81 “UBLKMOV”

With SFC 81 “UBLKMOV” (uninterruptible block move), you can copy the contents of a memory area (= source area) consistently to a different memory area (= destination area). The copy operation cannot be interrupted by other operating system activities.

SFC 81 “UBLKMOV” enables you to copy the following memory areas:

- Memory markers
- DB contents
- Process image of the inputs
- Process image of outputs

The maximum amount of data you can copy is 512 bytes. Take into consideration the restrictions for the specific CPU, which are documented in the operations list, for example.

Since copying cannot be interrupted, the interrupt reaction times of your CPU may increase when using SFC 81 “UBLKMOV”.

The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies as much data to the destination area as that contained in the source area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

1.13.1 Consistency for Communication Blocks and Functions

Using S7-400 the communication data is not processed in the scan cycle checkpoint; instead, this data is processed in fixed time slices during the program cycle.

In the system the byte, word and double word data formats can always be processed consistently, in other words, the transfer or processing of 1 byte, 1 word (= 2 bytes) or 1 double word (= 4 bytes) cannot be interrupted.

If communication blocks (such as SFB 12 “BSEND”) are called in the user program, which are only used in pairs (such as SFB 12 “BSEND” und SFB 13 “BRCV”) and which share access to data, the access to this data area can be coordinated between themselves, using the “DONE” parameter, for example. Data consistency of the communication areas transmitted locally with a communication block can thus be ensured in the user program.

S7 communication functions such as SFB 14 “GET”, SFB 15 “PUT” react differently because no block is needed in the user program of the destination device. In this case the size of data consistency has to be taken into account beforehand during the programming phase.

1.13.2 Access to the Working Memory of the CPU

The communication functions of the operating system access the working memory of the CPU in fixed block lengths. The block size is a variable length up to a maximum of 462 bytes.

1.13.3 Read from and Writing to a DP Standard Slave Consistently

Writing Data Consistently to a DP Standard Slave Using SFC 14 “DPRD_DAT”

Using SFC 14 “DPRD_DAT” (read consistent data of a DP standard slave) you can consistently read the data of a DP standard slave.

The data read is entered into the destination range defined by RECORD if no error occurs during the data transmission.

The destination range must have the same length as the one you have configured for the selected module with STEP 7.

By invoking SFC 14 you can only access the data of one module / DP ID at the configured start address.

1.13.4 Writing Data Consistently to a DP Standard Slave Using SFC 15 “DPWR_DAT”

Using SFC 15 “DPWR_DAT” (write consistent data to a DP standard slave) you can consistently write data to the DP standard slave addressed in the RECORD.

The source range must have the same length as the one you have configured for the selected module with STEP 7.

Note

The Profibus DP standard defines the upper limit for the transmission of consistent user data (see following section). Typical DP standard slaves adhere to this upper limit. In older CPUs (<1999) there are restrictions in the transmission of consistent user data depending on the CPU. For these CPUs you can determine the maximum length of the data which the CPU can consistently read and write to and from the DP standard in the respective technical specifications under the index entry “DP Master – User data per DP slave”. Newer CPUs are capable of exceeding the value for the amount of data that a DP standard slave can send and receive.

Upper Limit for the Transmission of Consistent User Data on a DP Slave

The Profibus DP standard defines the upper limit for the transmission of consistent user data to a DP slave. For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP slave.

During the configuration you can determine the size of the consistent area. You can set a maximum length of consistent data at 64 words = 128 bytes in the special identification format (SKF) (128 bytes for inputs and 128 bytes for outputs); the data block size cannot exceed this.

This upper limit only applies to pure user data. Diagnostics and parameter data are regrouped into full records and therefore always transferred consistently.

In the general identification format (AKF) the maximum length of consistent data can be set at 16 words = 32 bytes (32 bytes for inputs and 32 bytes for outputs); the data block size cannot exceed this.

Note in this context that a CPU 41x in a general environment acting as a DP slave on a third-party master (connection defined by GSD) has to be configured with the general identification format. The transfer memory of a CPU 41x acting as a DP slave to the PROFIBUS DP can therefore be a maximum of 16 words = 32 bytes.

1.13.5 Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs listed below. The data area of a DP slave that should transfer consistently is transferred to a process image partition. The information in this area are therefore always consistent. You can subsequently use load/transfer commands (such as L EW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

This applies to CPUs with firmware version 3.0 or later:

S7-400 CPU	MLFB
CPU 412-1	6ES7412-1XF03-0AB0
CPU 412-2	6ES7412-2XG00-0AB0
CPU 414-2	6ES7414-2XG03-0AB0
CPU 414-3	6ES7414-3XJ00-0AB0
CPU 416-2	6ES7416-2XK02-0AB0
CPU 416-3	6ES7416-3XL00-0AB0
CPU 417-4	6ES7417-4XL00-0AB0

No I/O access error occurs with direct access (e.g. L PEW or T PAW).

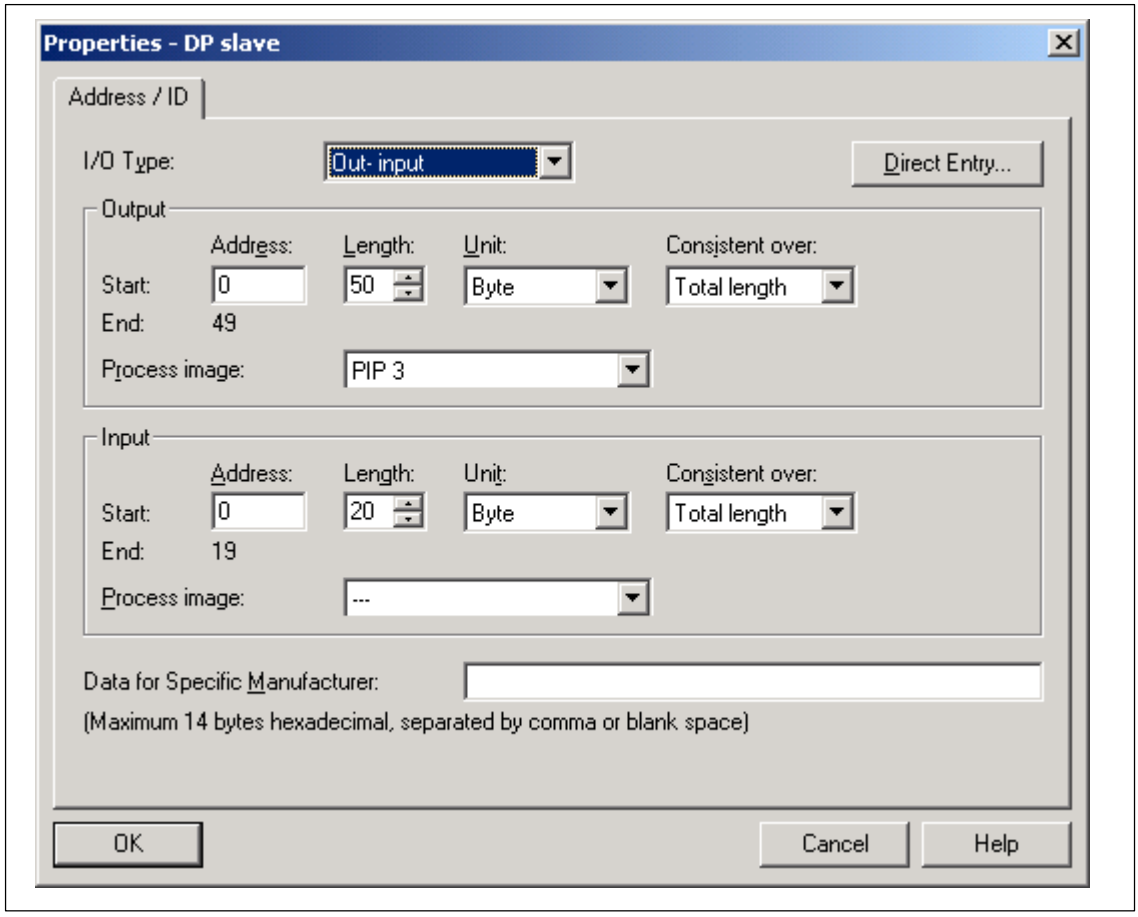
The following is important for converting from the SFC14/15 method to the process image method:

- When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- SFC 50 “RD_LGADR” outputs another address area with the SFC 14/15 method as with the process image method.
- If you are using a CP 443-5 ext the simultaneous use of SFC 14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Example:

The following example (of the process image partition 3 “TPA 3”) shows such a configuration in HW Config:

- TPA 3 at output: These 50 bytes are stored consistent in the process image partition 3 (pull-down list “Consistent over –> entire length”) and can therefore be read through the normal “load input xy” commands.
- Selecting “Process Image Partition –> ––” under input in the pull-down menu means: do not store in a process image. Then the handling can only be performed using the system functions SFC14/15.



Memory Concept and Startup Scenarios 2

Chapter Overview

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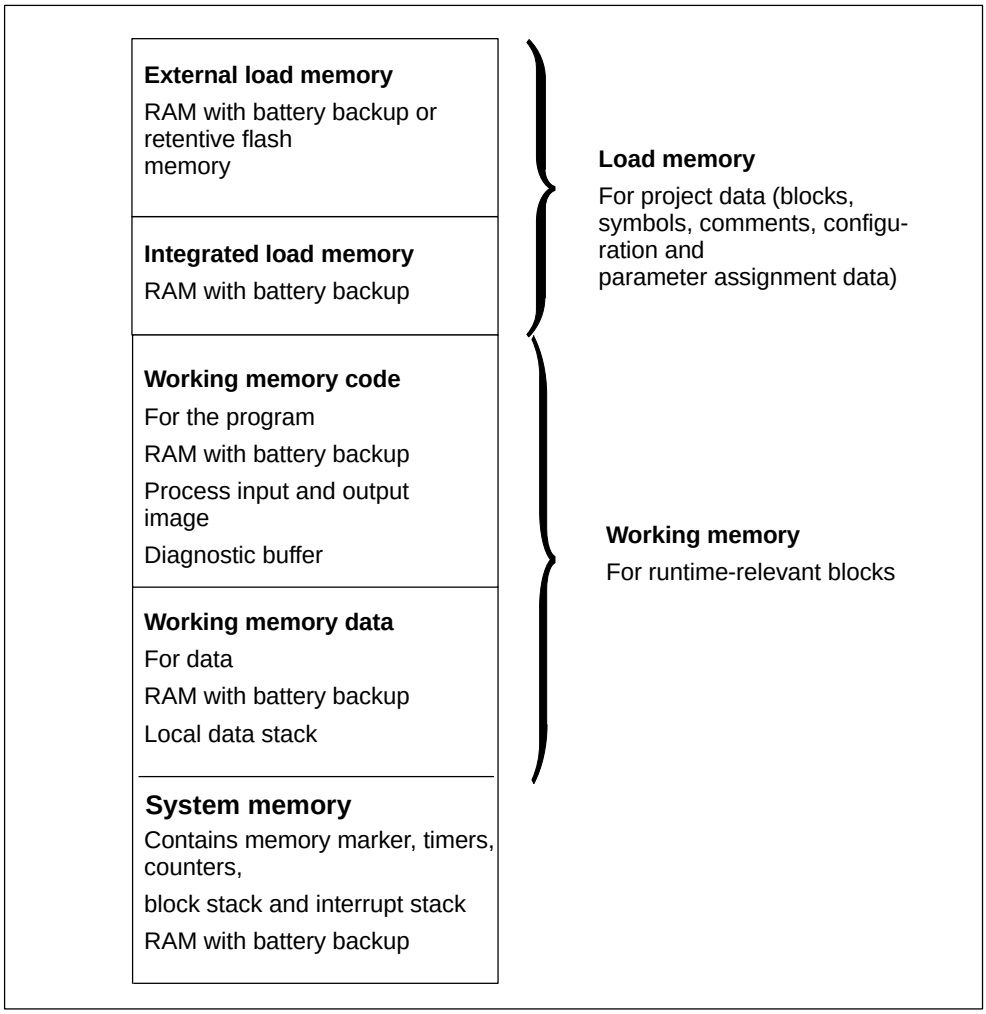
2.1	Overview of the Memory Concept of S7-400 CPUs	2-2
2.2	Overview of the Startup Scenarios for S7-400-CPUs	2-5

2.1 Overview of the Memory Concept of S7-400 CPUs

Subdivision of the Memory Areas

You can divide the memory of the S7 CPUs into the following areas:



Important Note for CPUs with Configurable Division of the Working Memory

If you use parameter assignment to change the division of the working memory, the working memory is reorganized when the system data are downloaded to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for code or data blocks is changed if you change the following parameters for loading the system data:

- Size of the process image (byte by byte; “Cycle/Clock Memory” tab)
- Communication resources (S7-400 only; “Memory” tab)
- Size of the diagnostic buffer (“Diagnostics/Clock” tab)
- Number of local data for all priority classes (“Memory” tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory in the CPU, you must take into consideration the following memory requirements when assigning parameters:

Table 2-1 Memory Requirements

Parameter	Required Working Memory	In Code/Data Memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of diagnostic buffer	20 bytes per entry in the diagnostic buffer	Code memory
Volume of local data	1 byte per byte of local data	Data memory

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Working memory for the runtime-relevant blocks (code blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as memory markers, timers, and counters. The system memory also receives the block stack and the interrupt stack.
- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program when a block is called for its temporary data. These data are only valid as long as the block is active.

  By changing the default values for the process image, local data, diagnostic buffer and communication resources (see the object properties of the CPU in HWCONFIG), you can control the working memory available to the runtime-relevant blocks.

Notice

Please note the following if you enlarge the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the enlarged process image. This particularly applies to IP and WF modules that you operate in the S5 adapter casing in a S7 400.

Flexible Memory Capacity

- Working memory:

  The capacity of the working memory is determined by selecting the appropriate CPU from the finely graded range of CPUs.

  In the case of the CPU 417, working memory can be expanded.
- Load memory:

  The integrated load memory is sufficient for small and medium-sized programs.

  The load memory can be increased for larger programs by inserting the RAM memory card.

  Flash memory cards are also available to ensure that programs are retained in the event of a power failure even if there isn't a backup battery. Flash memory cards can also be used (as of 2 MB for standard CPUs, as of 4 MB for fault-tolerant CPUs) to send and execute operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

2.2 Overview of the Startup Scenarios for S7-400-CPUs

Cold Restart

- At a cold restart, all the data (process image, memory markers, timers, counters and data blocks) are reset to the start values stored in the program (load memory) - irrespective of whether they were configured as retentive or non-retentive.
- Program processing is started from the beginning again (startup OB or OB 1).

Warm Restart

- At a warm restart, the process image and the non-retentive memory markers, timers and counters are reset.

  Retentive memory markers, timers and counters and all the data blocks retain their last valid value.
- Program processing is started from the beginning again (startup OB or OB 1).
- When the power supply is interrupted, a warm restart is only possible in backed-up mode.

Restart

- At a restart, all the data, including the process image, retain their last valid value.
- Program processing is resumed at exactly the instruction at which the interruption occurred.
- The outputs are not changed until the end of the current cycle.
- When the power supply is interrupted, a restart is only possible in backed-up mode.

Cycle and Reaction Times of the S7-400

3

This chapter explains the composition of the cycle and reaction times of the S7-400.

You can display the cycle time of your user program on the relevant CPU using the programming device (see manual *Configuring Hardware and Communication Connections with STEP 7 Version 5.0* or higher).

Examples will illustrate how you calculate the cycle time.

The reaction time is important for monitoring a process. This chapter provides a detailed description of how to calculate this. If you use a CPU 41x-2 DP as a master in the PROFIBUS DP network, you also have to take into account DP cycle times (see Section 3.5).

Chapter Overview

Further Information

You will find further information on the following processing times in the S7-400 Instruction List. It lists all the *STEP 7* instructions that can be processed by the relevant CPUs, together with their execution times and all the SFCs/SFBs integrated in the CPUs and the IEC functions that can be called in *STEP 7*, together with their processing times.

3.1 Cycle Time

In this chapter you will learn about the composition of the cycle time and how you can calculate the cycle time.

Definition of the Cycle Time

The cycle time is the time which the operating system needs to process a program run – in other words, an OB 1 run – and all the program segments and system activities that interrupt that run.

This time is monitored.

Time-Sharing Model

Cyclic program scanning, and thus also processing of the user program, is performed in time slices. So that you can better appreciate these processes, we will assume in the following that each time slice is exactly 1 ms long.

Process Image

The process signals are read or written prior to program scanning so that a consistent image of the process signals is available to the CPU for the duration of cyclic program scanning. Then the CPU does not directly access the signal modules during program scanning when the address area “inputs” (I) and “outputs” (O) are addressed, but addresses instead the internal memory area of the CPU on which the image of the inputs and outputs is located.

The Cyclic Program Scanning Process

The following table and figure illustrate the phases of cyclic program scanning.

Table 3-1 Cyclic Program Scanning

Step	Process
1	The operating system starts the scan cycle monitoring time.
2	The CPU writes the values from the process-image output table in the output modules.
3	The CPU reads out the status of the inputs at the input modules and updates the process-image input table.
4	The CPU processes the user program in time slices and performs the operations specified in the program.
5	At the end of a cycle, the operating system executes pending tasks, such asthe loading and clearing of blocks.
6	The CPU then goes back to the beginning of the cycle after the configured minimum cycle time, as necessary, and starts cycle time monitoring again.

Parts of the Cycle Time

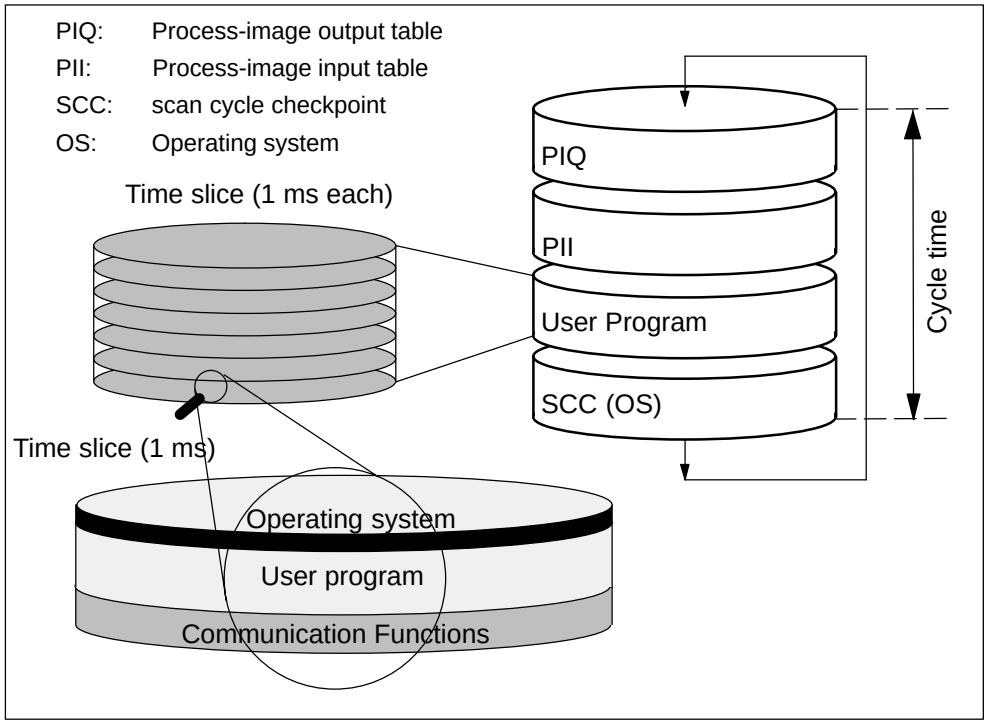


Figure 3-1 Parts and Composition of the Cycle Time

3.2 Cycle Time Calculation

Increasing the Cycle Time

Basically, you should note that the cycle time of a user program is increased by the following:

- Time-driven interrupt processing
- Hardware interrupt processing (see also Section 3.8)
- Diagnostics and error handling (see also Section 3.9)
- Communications via the MPI and CPs connected via the communication bus (for example, Ethernet, Profibus, DP); contained in the communication load
- Special functions such as control and monitoring of variables or block status
- Transfer and clearance of blocks, compression of the user program memory

Factors that Influence the Cycle Time

The following table indicates the factors that influence the cycle time.

Table 3-2 Factors that Influence the Cycle Time

Factors	Remark
Transfer time for the process-image output table (PIQ) and the process-image input table (PII)	... see Table 3-5
User program processing time	... is calculated from the execution times of the different instructions (see *S7-400 Instruction List*). For a special characteristic of the CPU 417-4H refer to Table 3-5.
Operating system scan time at scan cycle checkpoint	... see Table 3-6
Increase in the cycle time from communications	You set the maximum permissible cycle load expected for communication in % in *STEP 7* (manual *Programming with STEP 7 Version 5.0*). See Section 3.4.
Impact of interrupts on the cycle time	Interrupt can interrupt the user program at any time. ... see Table 3-7

Note
With CPUs produced prior to October 1998, updating of the process image of the outputs takes place before the scan cycle checkpoint.

Process Image Updating

The table below shows the CPU times for process image updating (process image transfer time). The times listed in the table are “ideal values” that may be increased by the occurrence of interrupts and by CPU communications.

The transfer time for process image updating is calculated as follows

C	+ portion in central rack (from line A of the following table)
	+ portion in expansion rack with local connection (from line B)
	+ portion in expansion rack with remote connection (from line C)
	+ portion via integrated DP interface (from line D)
	+ portion of consistent data via integrated DP interface (from line E1)
	+ portion of consistent data via external DP interface (from line E2)
	= transfer time for process image updating

The following tables list the individual portions of the transfer times for updating the process image (process image transfer time), once for standard CPUs and once for redundant CPUs. The times listed in the table are “ideal values” that may be increased by the occurrence of interrupts and by CPU communications.

Table 3-3 Portions of the process image transfer time

	Portions n = number of bytes in the process image c= number of consistency areas ****) in the process image	**CPU 412**	**CPU 414** **CPU 417**	**CPU 416**
C	Base load	30 µs	20 µs	18 µs
A	In the central rack *) **)	n * 1.9 µs	n * 1.9 µs	n * 1.9 µs
B	In the expansion rack with local connection **)	n * 5 µs	n * 5 µs	n * 5 µs
C	In the expansion rack with remote connection **) ***)	n * 10 µs	n * 10 µs	n * 10 µs
D	In the DP area for the integrated DP interface	n * 0.5 µs	n * 0.5 µs	n * 0.5 µs
E 1	Consistent data in the process image for the integrated DP interface	k * 40 µs + n * 0.5 µs	k * 27 µs + n * 0.5 µs	k * 22 µs + n * 0.5 µs
E 2	Consistent data in the process image for the external DP interface (CP 443-5 extended)	k * 40 µs + n * 3.2 µs	k * 27 µs + n * 3.2 µs	k * 22 µs + n * 2.1 µs

*) Also applies to the external DP interface (CP 443-5 extended)

**) In the case of I/O modules that are plugged into the central rack or an expansion rack, the specified value contains the runtime of the I/O module

***) Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

****) The areas set in HW Config that are written to or read from the I/O at once and are therefore consistent.

Table 3-4 Portions of the process image transfer time, H CPUs

	Portions n = number of bytes in the process image m= number of accesses to the process image *) c= number of consistency areas in the process image	**CPU 41x-4H single mode**	**CPU 41x-4H redundant**
C	Base load	20 µs	20 µs
A **)	In the central rack Read byte/word/double word Write byte/word/double word	 (m * 23 + n * 1.9) µs (m * 17 + n * 1.9) µs	 (m * 28 + n* 1.9) µs (m * 20 + n * 1.9) µs
B **)	In the expansion rack with local connection Read byte/word/double word Write byte/word/double word	 (m * 23 + n * 5) µs (m * 17 + n * 5) µs	 (m * 28 + n * 5) µs (m * 20 + n * 5) µs
C **) ***)	In the expansion rack with remote connectionRead byte/word/double word Write byte/word/double word	 (m * 23 + n * 10) µs (m * 17 + n * 10) µs	 (m * 28 + n * 10) µs (m * 20 + n * 10) µs
D	In the DP area of the integrated DP interfaceRead byte/word/double word Write byte/word/double word	 (m * 23 + n * 0.5) µs (m * 17 + n * 0.5) µs	 (m * 28 + n * 0.5) µs (m * 20 + n * 0.5 µs
E1	Consistent data in the process image for the integrated DP interface Reade data Write data	 (k * 50 + n * 0.6) µs (k * 50 + n * 0.6) µs	 (k * 100 + n * 1.2)µs (k * 100 + n * 0.6)µs
E2	Consistent data in the process image for the external DP interface (CP 443-5 extended) Read data Write data	 (k * 50 + n * 3.4) µs (k * 50 + n * 3.4) µs	 (k * 100 + n * 4.0)µs (k * 100 + n * 3.4)µs

*) The data of a module are updated with the minimal number of accesses.
(E.g.: For 8 bytes there are two double word accesses, for 16 bytes four 4 double word accesses.)

**) In the case of I/O modules that are plugged into the central rack or an expansion rack the specified value contains the runtime of the I/O module.

***) Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

Increasing the Cycle Time of the CPU 41x-4H

With the CPU 41x-4H, you must further multiply the calculated cycle time by a factor specific to the CPU in question. This factor is shown in the table below:

Table 3-5 User program processing time for the CPU 41x-4H

Process	CPU 41x-4H single mode	CPU 41x-4H redundant
Factor	1.03	1.14

Operating System Scan Time at the Scan Cycle Checkpoint

The table below lists the operating system scan times at the scan cycle checkpoint of the CPUs.

Table 3-6 Operating system scan time at scan cycle checkpoint

Process	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4	CPU 41x-4H single mode	CPU 41x-4H redundant
Scan cycle control at the SCC	240 µs	170 µs	135 µs	170 µs	190 -1770 µs ∅ 200 µs	395 - 1865 µs ∅ 445 µs

Increase in Cycle Time by Nesting Interrupts

Table 3-7 Increase in Cycle Time by Nesting Interrupts

CPU	Hardware Interrupt	Diagnostic Interrupt	Day Interrupt	Time-Delay Interrupt	Watchdog Interrupt	Programming/ Periphery Access Error
CPU 412-1/-2	520 µs	590 µs	490 µs	370 µs	370 µs	180 µs / 190 µs
CPU 414-2/-3	370 µs	420 µs	350 µs	260 µs	260 µs	130 µs / 140 µs
CPU 416-2/-3	300 µs	340 µs	280 µs	210 µs	210 µs	100 µs / 105 µs
CPU 417-4	370 µs	420 µs	350 µs	260 µs	260 µs	130 µs / 140 µs
CPU 41x-4 H single mode	390 µs	450 µs	310 µs	270 µs	255 µs	140 µs / 170 µs
CPU 41x-4 H redundant	705 µs	785 µs	560 µs	530 µs	530 µs	175 µs / 240 µs

You have to add the program execution time at the interrupt level to this increase.

If several interrupts are nested, their times must be added together.

3.3 Different Cycle Times

The length of the cycle time (T_{cyc}) is not identical in each cycle. The following figure shows different cycle times, T_{cyc1} and T_{cyc2}. T_{cyc2} is longer than T_{cyc1} , because the cyclically scanned OB 1 is interrupted by a time-of-day interrupt OB (in this instance, OB 10).

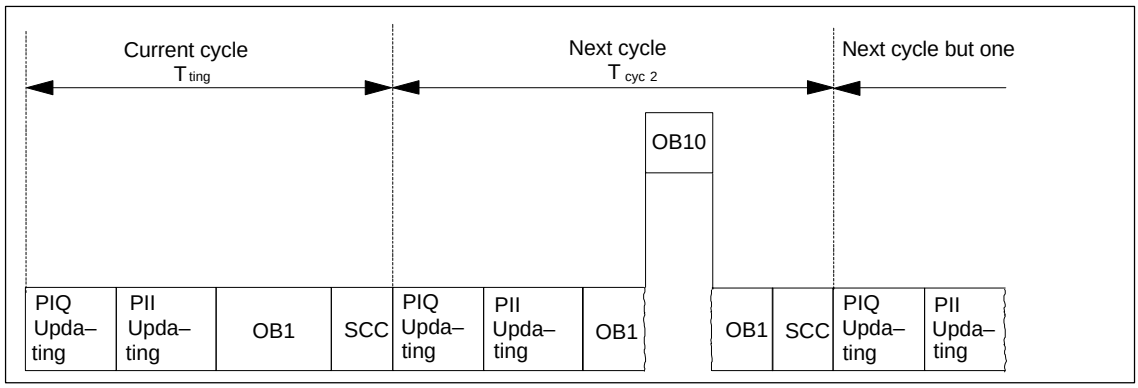


Figure 3-2 Different Cycle Times

A further reason for cycle times of different length is the fact that the execution time of blocks (for example, OB 1) can vary on account of:

- Conditional instructions
- Conditional block calls
- Different program paths
- Loops, etc.

Maximum Cycle Time

You can modify the default maximum cycle time in STEP 7 (cycle monitoring time). If this time has expired, OB 80 is called, and in it you can define how you want the CPU to respond to the time error. If you do not retrigger the cycle time with SFC 43, OB 80 doubles the cycle time at the first call. In this case, the CPU goes to STOP at the second call of OB 80.

If there is no OB 80 in the CPU memory, the CPU goes to STOP.

Minimum Cycle Time

You can set a minimum cycle time for a CPU in STEP 7. This is practical if

- you want the intervals of time between the start of program scanning of OB1 (free cycle) to be roughly of the same length, or
- updating of the process images would be performed unnecessarily often with too short a cycle time, or
- you want to process a program with the OB 90 in the background (not CPU 41x-4H).

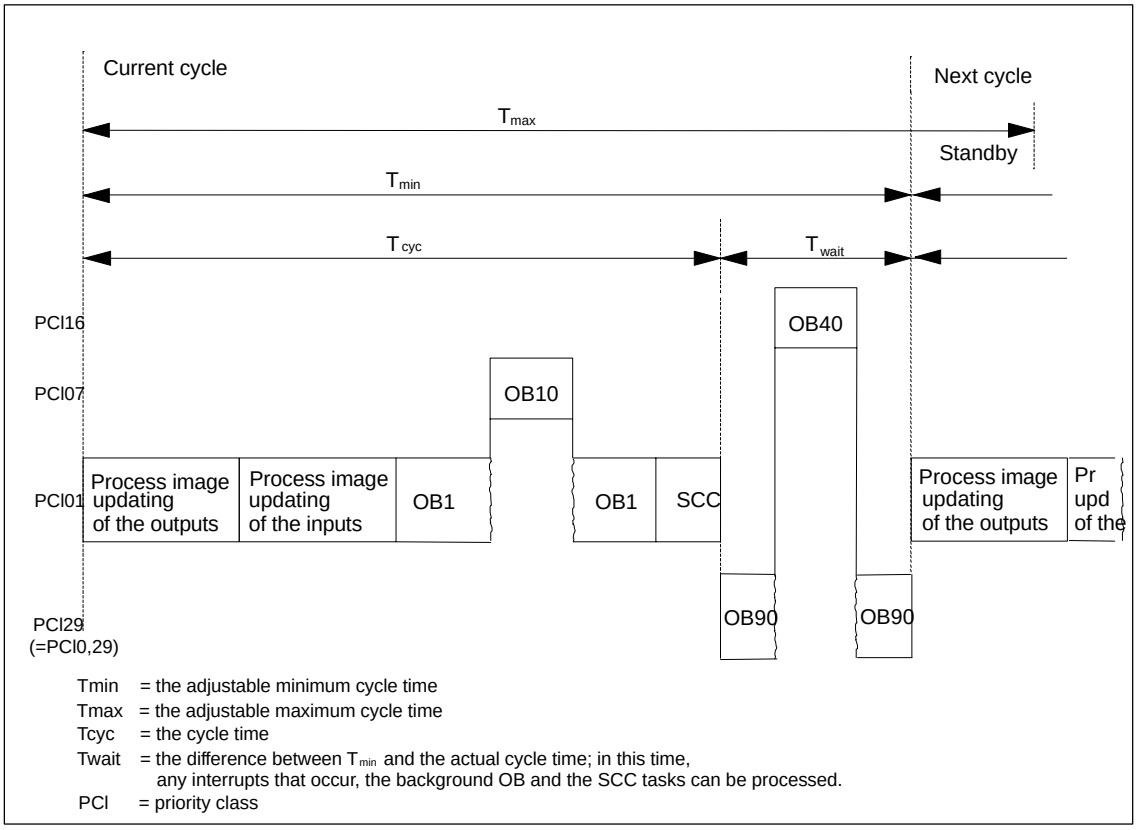


Figure 3-3 Minimum Cycle Time

The actual cycle time is the sum of T_{cyc} and T_{wait}. It is always greater than or equal to T_{min}.

3.4 Communication Load

The CPU operating system continually makes available to communications the percentage you configured for the overall CPU processing performance (time sharing). If this processing performance is not required for communications, it is available for other processing tasks.

In the hardware configuration, you can set the load due to communications to between 5% and 50%. By default, the value is set to 20%.

This percentage should be regarded as an average value, in other words, the communications component can be considerably greater than 20% in a time slice. On the other hand, the communications component in the next time slice is only a few or zero percent. This fact is also expressed by the following formula:

$$\text{Actual cycle time} = \text{cycle time} \times \frac{100}{100 - \text{"configured communication load in \%"}}$$

Round up the result to the next whole number !

Figure 3-4 Formula: Influence of Communication Load

Data consistency

The user program is interrupted for communications processing. The interrupt can be executed after any instruction. These communication jobs can modify the program data.
This means that the data consistency cannot be guaranteed for the duration of several accesses.
The manner in which you can guarantee consistency enduring for more than just one instruction is explained in the manual *System Software for S7-300/400 System and Standard Functions*, in the chapter on *Overview of S7 Communications and S7 Basic Communications*.

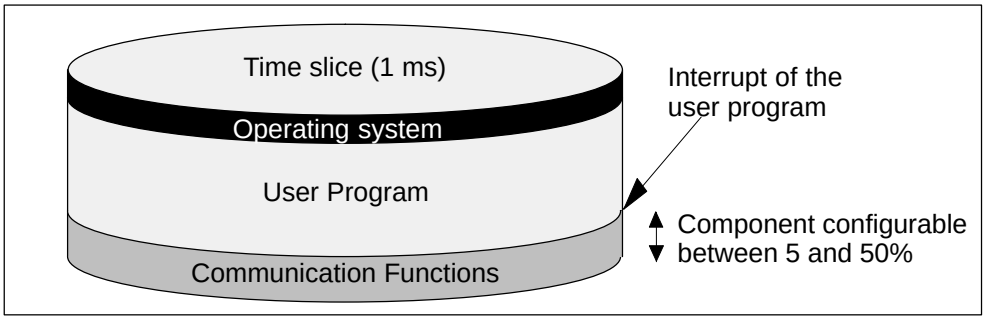


Figure 3-5 Breakdown of a Time Slice

Of the part remaining, the operating system of the S7-400 requires only a negligibly small amount for internal tasks.
CPU 41x-4H is an exception: For H CPUs the operating system part is taken into account in the factor specified in Table 3-5.

Example: 20 % Communication Load

You have configured a communication load of 20% in the hardware configuration.

The calculated cycle time is 10 ms.

A 20% communication load means that, on average, 200 µs and 800 µs of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 800 µs = 13 time slices to process one cycle. This means that the actual cycle time is 13 times a 1 ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

This means that 20% communications do not increase the cycle linearly by 2 ms but by 3 ms.

Example: 50 % Communication Load

You have configured a communication load of 50% in the hardware configuration.

The calculated cycle time is 10 ms.

This means that 500 µs of each time slice remain for the cycle. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 ms if the CPU fully utilizes the configured communication load.

A 50 % communication load means that, on average, 500 µs and 500 µs of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 times a 1 ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communications do not increase the cycle linearly by 5 ms but by 10 ms.

Dependency of the Actual Cycle Time on the Communication Load

The following figure describes the non-linear dependency of the actual cycle time on the communication load. As an example, we have chosen a cycle time of 10 ms.

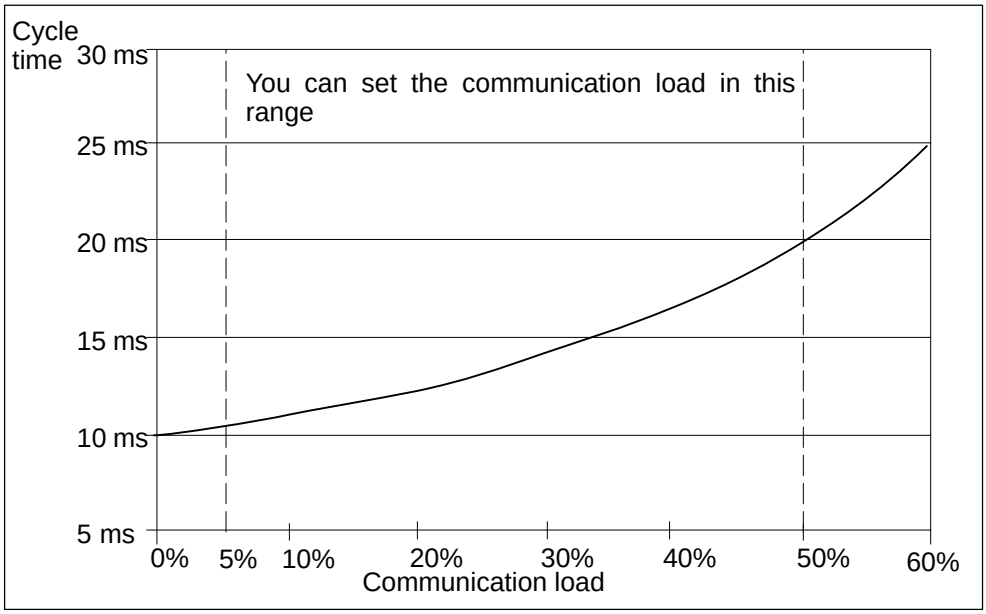


Figure 3-6 Dependency of the Cycle Time on the Communication Load

Further Effect on the Actual Cycle Time

Due to the increase in the cycle time as a result of the communications component, even more asynchronous events occur, from a statistical point of view, within an OB 1 cycle than, say, interrupts. This also increases the OB 1 cycle. This increase depends on how many events occur per OB 1 cycle and how long event processing lasts.

Notes

- Check the effects of a change of the value for the parameter “Cycle load due to communications” in system operation.
- The communication load must be taken into account when you set the maximum cycle time, since time errors will occur if it is not.

Recommendations

- If possible, apply the default value.
- Use a larger value only if the CPU is being used primarily for communication purposes and the user program is non-time-critical. In all other cases select a smaller value.

3.5 Reaction Time

Definition of the Reaction Time

The reaction time is the time from an input signal being detected to changing an output signal linked to it.

Variation

The actual reaction time is somewhere between a shortest and a longest reaction time. For configuring your system, you must always reckon with the longest reaction time.

The shortest and longest reaction times are analyzed below so that you can gain an impression of the variation of the reaction time.

Factors

The reaction time depends on the cycle time and on the following factors:

- Delay in the inputs and outputs
- Additional DP cycle times on the PROFIBUS-DP network
- Execution of the user program

Delay in the Inputs and Outputs

Depending on the module, you must heed the following time delays:

- For digital inputs: the input delay
- For interrupt-capable digital inputs: the input delay + the module-internal preparation time
- For digital outputs: negligible time delays
- For relay outputs: typical time delays from 10 to 20 ms. The delay of the relay outputs depends, among other things, on the temperature and voltage.
- For analog inputs: cycle time of analog input module
- For analog outputs: response time of the analog output module

The time delays can be found in the technical specifications of the signal modules.

DP Cycle Times on the PROFIBUS-DP Network

If you have configured your PROFIBUS-DP network with *STEP 7*, then *STEP 7* will calculate the typical DP cycle time that must be expected. You can then have the DP cycle time of your configuration displayed for the bus parameters on the programming device.

The following figure will provide you with an overview of the DP cycle time. We assume in this example that each DP slave has 4 byte of data on average.

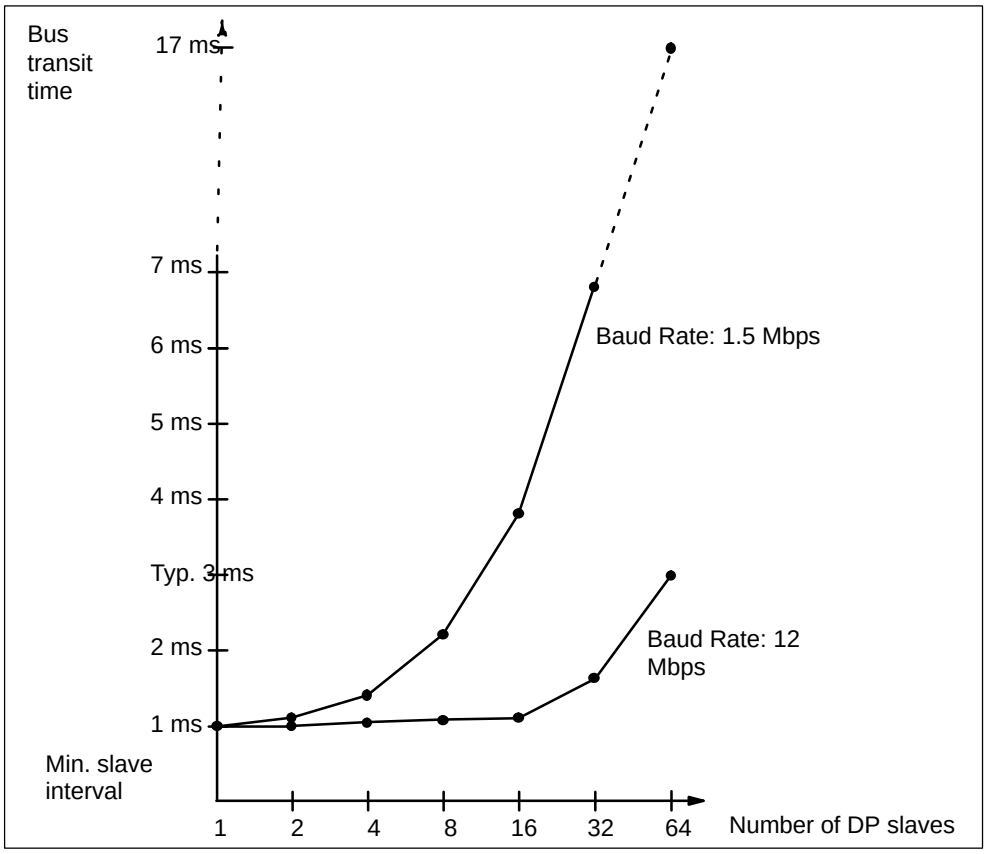


Figure 3-7
DP Cycle Times on the PROFIBUS-DP Network

If you are operating a PROFIBUS-DP network with more than one master, you must take the DP cycle time into account for each master. In other words, perform a separate calculation for each master and add the results together.

Shortest Reaction Time

The following figure illustrates the conditions under which the shortest reaction time is achieved.

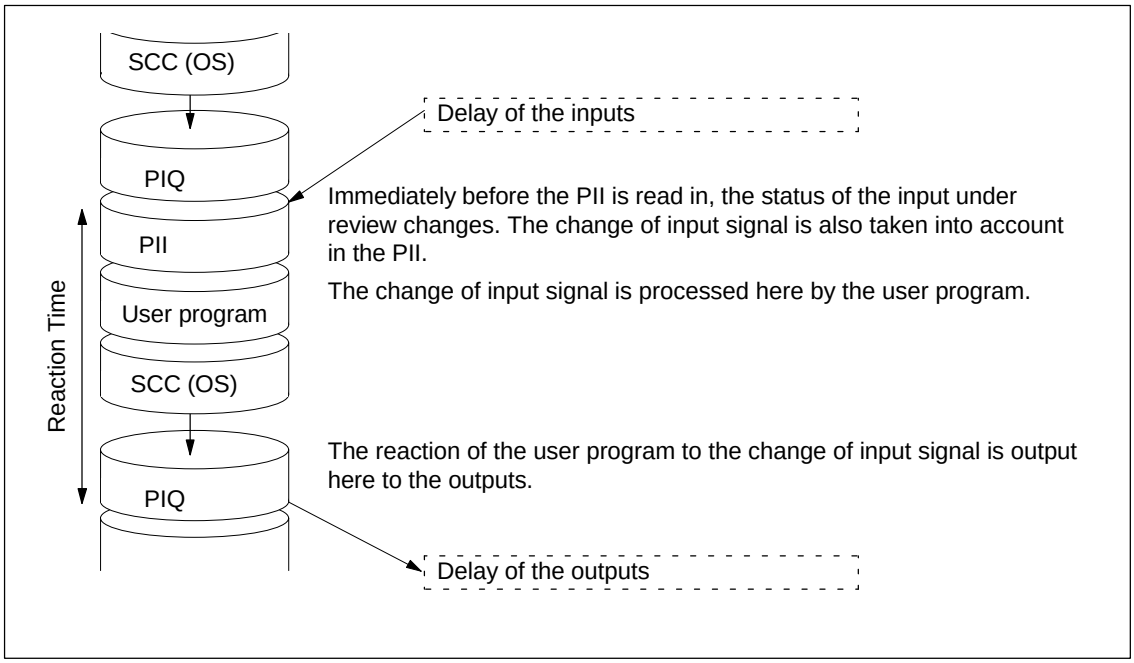


Figure 3-8 Shortest Reaction Time

Calculation

The (shortest) reaction time is made up as follows:

- 1 × process image transfer time of the inputs +
- 1 × process image transfer time of the outputs +
- 1 × program processing time +
- 1 × operating system processing time at SCC +
- Delay in the inputs and outputs

This is equivalent to the sum of the cycle time and the delay in the inputs and outputs.

Note

If the CPU and signal module are not in the central rack, you have to add double the runtime of the DP slave frame (including processing in the DP master).

Longest Reaction Time

The following figure shows you how the longest reaction time results.

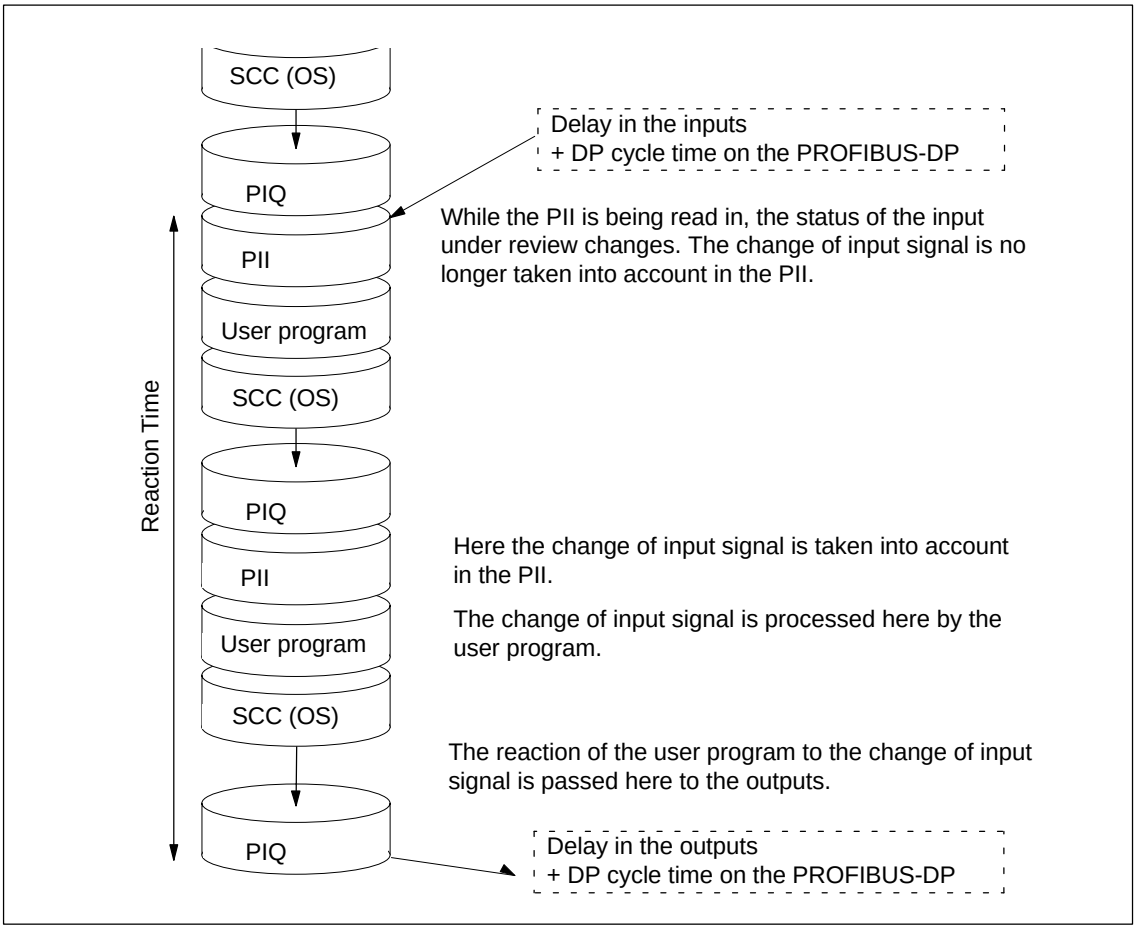


Figure 3-9 Longest Reaction Time

Calculation

The (longest) reaction time is made up as follows:

- 2 × process image transfer time of the inputs +
- 2 × process image transfer time of the outputs +
- 2 × operating system processing time +
- 2 × program processing time +
- 2 × runtime of the DP slave frame (including processing in the DP master) +
- Delay in the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.

I/O Direct Accesses

You can achieve faster reaction times by direct access to the I/O in the user program, for example with

- L PIB or
- T PQW

you can avoid the reaction times in part, as described above.

Reducing the Reaction Time

In this way the maximum reaction time is reduced to

- Delay in the inputs and outputs
- Runtime of the user program (can be interrupted by high-priority interrupt handling)
- Runtime of direct accesses
- Twice the bus transit time of DP

The following table lists the execution times of direct accesses by the CPU to I/O modules. The times shown are “ideal values”.

Table 3-8 Reducing the Reaction Time

Type of Access	CPU 412-1 412-2	CPU 414-2 414-3	CPU 416-2 416-3	CPU 417-4	CPU 41x-4H single mode	CPU 41x-4H redundant
Read byte	2.6 µs	2.1 µs	2.0 µs	2.4 µs	34 µs	64 µs
Read word	4.1 µs	3.5 µs	3.4 µs	3.8 µs	37 µs	67 µs
Read double word	8.0 µs	7.0 µs	6.7 µs	7.6 µs	41 µs	71 µs
Write byte	2.7 µs	2.2 µs	2.1 µs	2.4 µs	29 µs	58 µs
Write word	4.2 µs	3.7 µs	3.6 µs	3.9 µs	32 µs	61 µs
Write double word	8.3 µs	7.4 µs	7.1 µs	7.8 µs	36 µs	65 µs
Read byte in the expansion rack with local link	11.6 µs	10.6 µs	5.3 µs	10.6 µs	–	–
Read byte in the expansion rack with remote link	17.2 µs	16.2 µs	10.1 µs	16.2 µs	–	–

The specified times are merely CPU processing times and apply, unless otherwise stated, to signal modules in the central rack.

Note

You can similarly achieve fast reaction times by using hardware interrupts; refer to Section 3.8.

3.6 How Cycle and Reaction Times Are Calculated

Cycle time

1. Using the Instruction List, determine the runtime of the user program.
2. Calculate and add the transfer time for the process image. You will find guide values for this in Table 3-3.
3. Add to it the processing time at the scan cycle checkpoint. You will find guide values for this in Table 3-6.
4. CPU 417-4H: Multiply the calculated value by the factor in Table 3-5.

The result you achieve is the cycle time.

Increasing the Cycle Time with Communication and Interrupts

5. Multiply the result by the following factor:

$$\frac{100}{100 - \text{“configured communication load in \%”}}$$

6. Using the Instruction List, calculate the runtime of the program sections that hardware interrupts. Add to it the relevant value in Table 3-7.
   Multiply this value by the factor from step 4.
   Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result you obtain is approximately the actual cycle time. Make a note of the result.

Table 3-9 Example of Calculating the Reaction Time

Shortest Reaction Time	Longest Reaction Time
7. Then, calculate the delays in the inputs and outputs and, if applicable, the DP cycle times on the PROFIBUS DP network.	7. Multiply the actual cycle time by a factor of 2.
	8. Then, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.
8. The result you obtain is the shortest reaction time.	9. The result you obtain is the longest reaction time.

3.7 Examples of Calculating the Cycle Time and Reaction Time

Example I

You have installed an S7-400 with the following modules in the central rack:

- One CPU 414-2
- Two digital input modules SM 421; DI 32×DC 24 V (4 byte each in PA)
- Two digital output modules SM 422; DO 32×DC 24 V/0.5A (4 byte each in PA)

User Program

According to the Instruction List, your user program has a runtime of 15 ms.

Cycle Time Calculation

The cycle time for the example results from the following times:

- Since the CPU-specific factor is 1.0, the user program processing time remains:

  approx. **15.0 ms**

- Process image transfer time

  Process image: 20 µs + 16 byte×1.9 µs = approx. **0.05 ms**

- Operating system runtime at scan cycle checkpoint:
  approx. **0.17 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 15.0 ms + 0.05 ms + 0.17 ms **= 15.22 ms.**

Calculation of the Actual Cycle Time

- Allowance of the communication load (default value: 20%):
  15.22 ms * 100 / (100-20) **= 19.03 ms.**
- There is no interrupt handling.

Rounded off, the actual cycle time is thus **19 ms.**

Calculation of the Longest Reaction Time

- Longest reaction time
  19.03 ms * 2 **= 38.06 ms.**
- The delay in the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt handling.

Rounded off, the longest reaction time is thus **= 38 ms.**

Example II

You have installed an S7-400 with the following modules:

- One CPU 414-2
- Four digital input modules SM 421; DI 32×DC 24 V (4 byte each in PA)
- Three digital output modules SM 422; DO 16×DC 24 V/2A (2 byte each in PA)
- Two analog input modules SM 431; AI 8×13 bit (not in PA)
- Two analog output modules SM 432; AO 8×13 bit (not in PA)

CPU Parameters

The CPU has been assigned parameters as follows:

- Cycle load due to communications: 40%

User Program

According to the Instruction List, the user program has a runtime of 10.0 ms.

Cycle Time Calculation

The theoretical cycle time for the example results from the following times:

- Since the CPU-specific factor is 1.0, the user program processing time remains:

  approx. **10.0 ms**
- Process image transfer time

  Process image: 20 µs + 22 byte×1.9 µs = approx. **0.06 ms**
- Operating system runtime at scan cycle checkpoint:
  approx. **0.17 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 10.0 ms + 0.06 ms + 0.17 ms **= 10.23 ms.**

Calculation of the Actual Cycle Time

- Allowance of communication load:
  10.23 ms * 100 / (100-40) **= 17.05 ms.**
- A time-of-day interrupt having a runtime of 0.5 ms is triggered every 100 ms. The interrupt cannot be triggered more than once during a cycle:
  0.5 ms + 0.35 ms (in Table 3-7) **= 0.85 ms.**
  Allowance for communication load:
  0.85 ms * 100 / (100-40) **= 1.42 ms.**
- 17.05 ms + 1.42 ms **= 18.47 ms.**

The actual cycle time is therefore **19 ms taking into account the time slices.**

Calculation of the Longest Reaction Time

- Longest reaction time
  19 ms * 2 **= 38 ms.**
- Delays in the inputs and outputs
  - The digital input module SM 421; DI 32×DC 24 V has an input delay of not more than **4,8 ms** per channel
  - The digital output module SM 422; DO 16×DC 24 V/2A has a negligible output delay.
  - The analog input module SM 431; AI 8×13 bit was assigned parameters for 50 Hz interference frequency suppression. This results in a conversion time of 25 ms per channel. Since 8 channels are active, a cycle time of **200 ms** results for the analog input module.
  - Analog output module SM 432; AO 8×13 bit was assigned parameters for the measuring range from 0 to 10V. This results in a conversion time of **0.3 ms** per channel. Since 8 channels are active, a cycle time of 2.4 ms results. To this must be added the settling time for the resistive load, which is 0.1 ms. A response time of **2.5 ms** therefore results for an analog output.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- **Case 1:** When a digital signal is read in, an output channel of the digital output module is set. This produces a reaction time of:

  Reaction time= 38 ms + 4.8 ms **= 42.8 ms**.
- **Case 2:** An analog value is read in and an analog value output. This produces a reaction time of:

  Reaction time = 38 ms + 200 ms + 2.5 ms **= 240.5 ms**.

3.8 Interrupt Reaction Time

Definition of the Interrupt Reaction Time

The interrupt reaction time is the time from when an interrupt signal first occurs to calling the first instruction in the interrupt OB.

The following general rule applies: Interrupts having a higher priority take precedence. This means that the interrupt reaction time is increased by the program processing time of the higher priority interrupt OBs and interrupt OBs with the same priority that have not yet been processed (queue).

Note
The interrupt reaction times can be delayed by read and write jobs with a high data volume (approx. 460 byte).
When interrupts are transferred between a CPU and DP master, only a diagnostic **or** hardware interrupt can be currently reported at any time from a DP line.

Calculation

	Min. interrupt reaction time of the CPU		Max. interrupt reaction time of the CPU
+	min. interrupt reaction time of the signal modules	+	max. interrupt reaction time of the signal modules
+	DP cycle time on PROFIBUS-DP	+	2 * DP cycle time on PROFIBUS-DP
=	Shortest Reaction Time	=	Longest Reaction Time

Figure 3-10 Calculating the Interrupt Reaction Time

Hardware Interrupt and Diagnostic Interrupt Reaction Times of CPUs

Table 3-10 Hardware Interrupt and Diagnostic Interrupt Reaction Times; Maximum Interrupt Reaction Time Without Communication

CPU	Hardware Interrupt Reaction Times		Diagnostic Interrupt Reaction Times	
	Min.	Max.	Min.	Max.
412-1/-2	360 µs	610 µs	440 µs	690 µs
414-2/-3	255 µs	435 µs	310 µs	490 µs
416-2/-3	210 µs	350 µs	250 µs	400 µs
417-4	255 µs	435 µs	310 µs	490 µs
41x-4H single mode	270 µs	530 µs	325 µs	645 µs
41x-4H redundant	375 µs	690 µs	415 µs	780 µs

Increasing the Maximum Interrupt Reaction Time with Communication

The maximum interrupt reaction time increases when communication functions are active. The increase is calculated with the following formula:

CPU 412: tv = 200 µs + 1000 µs × n%

CPU 414-417: tv = 100 µs + 1000 µs × n%

CPU 41x-4H tv = 100 µs + 1000 µs × n%, considerable more time possible

where n = cycle load from communication

Signal Modules

The hardware interrupt reaction time of the signal modules is made up as follows:

- Digital input modules

  Hardware interrupt reaction time = internal interrupt processing time + input delay

  You will find the times in the data sheet of the digital input module concerned.

- Analog input modules

  Hardware interrupt reaction time = internal interrupt processing time + conversion time

  The internal interrupt processing time of the analog input modules is negligible. The conversion times can be taken from the data sheet of the analog input module concerned.

The diagnostic interrupt reaction time of the signal modules is the time which elapses between a diagnostics event being detected by the signal module and the diagnostic interrupt being triggered by the signal module. This time is so small that it can be ignored.

Hardware Interrupt Processing

When the hardware interrupt OB 40 is called, the hardware interrupt is processed. Interrupts with higher priority interrupt hardware interrupt processing, and direct access to the I/O is made when the instruction is executed. When hardware interrupt processing is completed, either cyclic program processing is continued or other interrupt OBs with the same or a lower priority are called and processed.

3.9 Example of Calculating the Interrupt Reaction Time

Parts of the Interrupt Reaction Time

As a reminder, the hardware interrupt reaction time is made up of the following:

- Hardware interrupt reaction time of the CPU
- Hardware interrupt reaction time of the signal module.
- 2 × DP cycle time on the PROFIBUS-DP

Example: You have an S7-400 consisting of a CPU 416-2 and 4 digital modules in the central rack. One digital input module is the SM 421; DI 16×UC 24/60 V; with hardware and diagnostic interrupts. In the parameter assignment of the CPU and the SM, you have only enabled the hardware interrupt. You do not require time-driven processing, diagnostics and error handling. You have assigned an input delay of 0.5 ms for the digital input module. No activities at the scan cycle checkpoint are required. You have set a cycle load from communication of 20%.

Calculation

The hardware interrupt reaction time for the example results from the following times:

- Hardware interrupt reaction time of the CPU 416-2: approx. 0.35 ms
- Increase from communication in accordance with the formula shown in the footnote of Table 3-10 :

  $$100\ \mu s + 1000\ \mu s \times 20\% = 300\ \mu s = 0.3\ ms$$

- Hardware interrupt reaction time of the SM 421; DI 16×UC 24/60 V:
  - Internal interrupt processing time: 0.5 ms
  - Input delay: 0.5 ms
- Since the signal modules are plugged into the central rack, the DP cycle time on the PROFIBUS-DP is not relevant.

The hardware interrupt reaction time results from the sum of the listed times:

Hardware interrupt reaction time = 0.35 ms +0.3 ms + 0.5 ms + 0.5 ms = approx. **1.65 ms**.

This calculated hardware interrupt reaction time is the time from a signal being applied across the digital input to the first instruction in OB 40.

3.10 Reproducibility of Time-Delay and Watchdog Interrupts

Definition of “Reproducibility”

Time-delay interrupt:

The deviation with time from the first instruction of the interrupt OB being called to the programmed interrupt time.

Watchdog interrupt

The variation in the time interval between two successive calls, measures between the first instruction of the interrupt OB in each case.

Reproducibility

Table 3-11 contains the reproducibility of time-delay and watchdog interrupts of the CPUs.

Table 3-11 Reproducibility of Time-Delay and Watchdog Interrupts of the CPUs.

Baugruppe	Reproducibility	
	Time-Delay Interrupt:	Watchdog Interrupt
CPU 412-1/-2	–770 µs / +330 µs	–40 µs / +40 µs
CPU 414-2/-3	–770 µs / +330 µs	–40 µs / +40 µs
CPU 416-2/-3	–770 µs / +330 µs	–40 µs / +40 µs
CPU 417-4	–770 µs / +330 µs	–40 µs / +40 µs
CPU 41x-4H single mode	–750 µs / +400 µs	–850 µs / +850 µs
CPU 41x-4H redundant	–500 µs / +800 µs	–700 µs / +700 µs

These times apply only if the interrupt can be executed at this time and not, for example, delayed by interrupts with higher priority or interrupts of identical priority that have not yet been executed.

Technical Specifications

4

Chapter overview

4.1 Technical Specifications of the CPU 412-1; (6ES7412-1XF03-0AB0)

CPU and Version	
MLFB	6ES7412-1XF03-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	48 Kbytes for code 48 Kbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.2 µs
• Word instructions	Min. 0.2 µs
• Integer math instructions	Min. 0.2 µs
• Floating-point math instructions	Min. 0.6 µs
Timers/Counters and Their Retentivity	
S7 counters	256
• Retentivity can be set	From Z 0 to Z 255
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	256
• Retentivity can be set	From T 0 to T 255
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	4 Kbytes
• Retentivity can be set	From MB 0 to MB 4095
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 511 (DB 0 reserved)
• Size	Max. 48 Kbytes
Local data (can be set)	Max. 8 Kbytes
• Preset	4 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 48 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 256
• Size	Max. 48 Kbytes
FCs	Max. 256
• Size	Max. 48 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	4 Kbytes/4 Kbytes
• Of which distributed MPI/DP interface	2 Kbytes/2 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 is assigned.	
Process Image	4 Kbytes/4 Kbytes (can be set)
• Preset	128 bytes/128 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	32768/32768
• Of which central	32768/32768
Analog channels	2048/2048
• Of which central	2048/2048

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	1
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the	CP 443-5 Extended
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• PROFIBUS and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	None
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 256
• Number of additional values per message	1
– With 100 ms grid	None
– With 500, 1000 ms grid	1
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 70
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 300
• Preset	150
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	4

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 64
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	16 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	16, with each of them reserved for PG and OPrespectively
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 bytes
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 16 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave

MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Constant bus cycle time	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 100 + number of slaves < 11
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
CiR synchronization time	
Base load	100 ms
Time per I/O byte	200 µs

Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	Approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 40 µA Max. 300 µA
maximum backup time	approx 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

4.2 Technical Specifications of the CPU 412-2; (6ES7412-2XG00-0AB0)

CPU and Version	
MLFB	6ES7412-2XG00-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	72 Kbytes for code
	72 Kbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.2 µs
• Word instructions	Min. 0.2 µs
• Integer math instructions	Min. 0.2 µs
• Floating-point math instructions	Min. 0.6 µs
Timers/Counters and Their Retentivity	
S7 counters	256
• Retentivity can be set	From Z 0 to Z 255
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	256
• Retentivity can be set	From T 0 to T 255
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	4 Kbytes
• Retentivity can be set	From MB 0 to MB 4095
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 511 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 8 Kbytes
• Preset	4 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 256
• Size	Max. 64 Kbytes
FCs	Max. 256
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	4 Kbytes/4 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	4 Kbytes/4 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61/62 is assigned.	
Process Image	4 Kbytes/4 Kbytes (can be set)
• Preset	128 bytes/128 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	32768/32768
• Of which central	32768/32768
Analog channels	2048/2048
• Of which central	2048/2048

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 3
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	None
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 256
• Number of additional values per message	1
– With 100 ms grid	None
– With 500, 1000 ms grid	1
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 70
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 300
• Preset	150
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	4

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Quantity	Max. 64
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 400 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	16 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	16, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and FC AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 16 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave

MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 64
• Address area	Max. 4 Kbytes inputs / 4 Kbytes outputs
• User data per DP slave	Max. 244 bytes inputs / 244 bytes outputs
DP slave	
Technical specifications as for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1

System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 100 + number of slaves < 11
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 40 µA Max. 320 µA
maximum backup time	approx 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.3 Technical Specifications of the CPU 414-2; (6ES7414-2XG03-0AB0)

CPU and Version	
MLFB	6ES7414-2XG03-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	128 Kbytes for code 128 Kbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.1 µs
• Word instructions	Min. 0.1 µs
• Integer math instructions	Min. 0.1 µs
• Floating-point math instructions	Min. 0.6 µs
Timers/Counters and Their Retentivity	
S7 counters	256
• Retentivity can be set	From Z 0 to Z 255
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	256
• Retentivity can be set	From T 0 to T 255
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	8 Kbytes
• Retentivity can be set	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 16 Kbytes
• Preset	8 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	8 Kbytes/8 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	6 Kbytes/6 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61/62 is assigned.	
Process Image	8 Kbytes/8 Kbytes (can be set)
• Preset	256 bytes/256 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	65536/65536
• Of which central	65536/65536
Analog channels	4096/4096
• Of which central	4096/4096

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs, LANs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	Max. 128
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 512
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 100
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 600
• Preset	300
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 256
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 400 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	31 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and FC AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave

MPI	
Utilities	
• Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 96
• Address area	Max. 6 Kbytes inputs/6 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
System function blocks (SFB)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 20
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 40 µA Max. 380 µA
maximum backup time	approx. 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.4 Technical Specifications of the CPU 414-3; (6ES7414-3XJ00-0AB0)

CPU and Version	
MLFB	6ES7414-3XJ00-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	384 Kbytes for code 384 Kbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.1 µs
• Word instructions	Min. 0.1 µs
• Integer math instructions	Min. 0.1 µs
• Floating-point math instructions	Min. 0.6 µs
Timers/Counters and Their Retentivity	
S7 counters	256
• Retentivity can be set	From Z 0 to Z 255
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	256
• Retentivity can be set	From T 0 to T 255
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	8 Kbytes
• Retentivity can be set	From MB 0 to MB 8191
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 16 Kbytes
• Preset	8 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	8 Kbytes/8 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	6 Kbytes/6 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 to OB 63 is assigned.	
Process Image	8 Kbytes/8 Kbytes (can be set)
• Preset	256 bytes/256 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	65536/65536
• Of which central	65536/65536
Analog channels	4096/4096
• Of which central	4096/4096

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 8
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 512
– 100 ms grid	Max. 128
– 500 ms grid	Max. 256
– 1000 ms grid	Max. 512
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 100
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 600
• Preset	300
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 256
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	31 without message processing, 8 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packages	
– Sender	Max. 8
– Receiver	Max. 16
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and FC AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	16

Functionality	
• PROFIBUS DP	DP master/DP slave
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 96
• Address area	Max. 6 Kbytes inputs/6 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1

System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 20
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 1.07 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 AMax. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ 40 µA Max. 420 µA
maximum backup time	approx 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.5 Technical Specifications of the CPU 416-2; (6ES7416-2XK02-0AB0, 6ES7416-2FK02-0AB0)

CPU and Version	
MLFB	6ES7416-2XK02-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	0.8 Mbytes for code 0.8 Mbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.08 µs
• Word instructions	Min. 0.08 µs
• Integer math instructions	Min. 0.08 µs
• Floating-point math instructions	Min. 0.48 µs
Timers/Counters and Their Retentivity	
S7 counters	512
• Retentivity can be set	From Z 0 to Z 511
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	512
• Retentivity can be set	From T 0 to T 511
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 32 Kbytes
• Preset	16 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61/62 is assigned.	
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	512 bytes/512 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	131072/131072
• Of which central	131072/131072
Analog channels	8192/8192
• Of which central	8192/8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 200
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 12 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave

MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/ 2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32
Functionality	
• PROFIBUS DP	DP Master
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 26
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 40 µA Max. 420 µA
maximum backup time	approx 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.6 Technical Specifications of the CPU 416-3; (6ES7416-3XL00-0AB0)

CPU and Version	
MLFB	6ES7416-3XL00-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	1.6 Mbytes for code
	1.6 Mbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.08 µs
• Word instructions	Min. 0.08 µs
• Integer math instructions	Min. 0.08 µs
• Floating-point math instructions	Min. 0.48 µs
Timers/Counters and Their Retentivity	
S7 counters	512
• Retentivity can be set	From Z 0 to Z 511
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	512
• Retentivity can be set	From T 0 to T 511
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data area (incl. memory markers, timers, counters)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 32 Kbytes
• Preset	16 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 to OB 63 is assigned.	
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	512 bytes/512 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	131072/131072
• Of which central	131072/131072
Analog channels	8192/8192
• Of which central	8192/8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 200
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 12 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps

DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
– Of which reserved	1 for programming device, 1 for OP
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, maximum 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes inputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32
Functionality	
• PROFIBUS DP	DP master/DP slave
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps

• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1

System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 26
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 1.07 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.6 A Max. 1.8 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 50 µA Max. 460 µA
maximum backup time	approx 332 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 8 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.7 Technical Specifications of the CPU 417-4; (6ES7417-4XL00-0AB0)

CPU and Version	
MLFB	6ES7417-4XL00-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	2 Mbytes for code
	2 Mbytes for data
• Expandable	Up to 10 Mbytes for code
	Up to 10 Mbytes for data
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.1 µs
• Word instructions	Min. 0.1 µs
• Integer math instructions	Min. 0.1 µs
• Floating-point math instructions	Min. 0.6 µs
Timers/Counters and Their Retentivity	
S7 counters	512
• Retentivity can be set	From Z 0 to Z 511
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	512
• Retentivity can be set	From T 0 to T 511
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 8191 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 64 Kbytes
• Preset	32 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 6144
• Size	Max. 64 Kbytes
FCs	Max. 6144
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61 to OB 64 is assigned.	
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	1024 bytes/1024 bytes
• Number of partial process images	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	131072/131072
• Of which central	131072/131072
Analog channels	8192/8192
• Of which central	8192/8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	2
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 16
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 200
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 10000
• Preset	1200
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	64

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

Communication Functions	
Programming device/OP communication	Yes
Number of connectable OPs	63 without message processing, 16 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for PG and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packages	
– Sender	Max. 16
– Receiver	Max. 32
• Size of GD packages	Max. 64 bytes
– Of which consistent	1 variable
S7 basic communication	Yes
• User data per job	Max. 76 bytes
– Of which consistent	16 Byte
S7 communication	Yes
• User data per job	Max. 64 Kbytes
– Of which consistent	1 variable (462 bytes)
S5-compatible communication	Yes (via CP – max. 10 – and FC AG_SEND and FC AG_RECV)
• User data per job	Max. 8 Kbytes
– Of which consistent	240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Interfaces	
1st Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	MPI: 44 DP: 32
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
MPI	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Global data communication	Yes
– S7 basic communication	Yes
– S7 communication	Yes
• Transmission rates	Up to 12 Mbps
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 32
• Address area	Max. 2 Kbytes inputs/2 Kbytes outputs
• User data per DP slave	Maximum 244 bytes E, 244 bytes A, distributed over 244 slots each with 128 bytes
DP slave	
• Utilities	
– Monitor/modify	Yes, if the interface is active
– Programming	Yes, if the interface is active
– Routing	Yes, if the interface is active
• DDB (GSD) file	http://www.ad.siemens.de/csi_e/gsd
• Transmission rate	Up to 12 Mbps
• Intermediate memory	244 bytes inputs/ 244 bytes outputs
– Address areas	Max. 32
– User data per address area	Max. 32 bytes
– Of which consistent	32 bytes
2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32
Functionality	
• PROFIBUS DP	DP master/DP slave
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125

• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
3rd Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
4th Interface	
Type of interface	Plug-in interface submodule
Insertable interface submodule	IF-964-DP
Technical features as for the 2nd interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 20
Equidistance	Yes
Shortest clock pulse	5 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	50×290×219
Slots required	2
Weight	approx. 1.07 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.8 AMax. 2.0 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typically 75 µA Maximum 860 µA
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
maximum backup time	approx 285 days
Power loss	Typ. 9 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.

4.8 Technical Specifications of the Memory Cards

Name	Order Number	Current Consumption at 5 V	BackupCurrents	Can Be Used in M7-400
MC 952 / 64 Kbytes / RAM	6ES7952-0AF00-0AA0	Typ. 20 mA Max. 50 mA	Typ. 0.5 µA Max. 20 µA	–
MC 952 / 256 Kbytes / RAM	6ES7952-1AH00-0AA0	Typ. 35 mA Max. 80 mA	typ. 1 µA Max. 40 µA	–
MC 952 / 1 Mbyte / RAM	6ES7952-1AK00-0AA0	Typ. 40 mA Max. 90 mA	Typ. 3 µA Max. 50 µA	–
MC 952 / 2 Mbytes / RAM	6ES7952-1AL00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA	–
MC 952 / 4 MB / RAM	6ES7952-1AM00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA	–
MC 952 / 8 MB / RAM	6ES7952-1AP00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA	–
MC 952 / 16 MB / RAM	6ES7952-1AS00-0AA0	Typ. 45 mA Max. 100 mA	Typ. 5 µA Max. 60 µA	–
MC 952 / 64 Kbytes / 5V Flash	6ES7952-0KF00-0AA0	Typ. 15 mA Max. 35 mA	–	–
MC 952 / 256 Kbytes / 5V Flash	6ES7952-0KH00-0AA0	Typ. 20 mA Max. 45 mA	–	–
MC 952 / 1 Mbyte / 5V Flash	6ES7952-1KK00-0AA0	Typ. 40 mA Max. 90 mA	–	Yes
MC 952 / 2 Mbytes / 5V Flash	6ES7952-1KL00-0AA0	Typ. 50 mA Max. 100 mA	–	Yes
MC 952 / 4 Mbytes / 5V Flash	6ES7952-1KM00-0AA0	Typ. 40 mA Max. 90 mA	–	Yes
MC 952 / 8 Mbytes / 5V Flash	6ES7952-1KP00-0AA0	Typ. 50 mA Max. 100 mA	–	Yes
MC 952 / 16 Mbytes / 5V Flash	6ES7952-1KS00-0AA0	Typ. 55 mA Max. 110 mA	–	Yes
MC 952 / 32 Mbytes / 5V Flash	6ES7952-1KT00-0AA0	Typ. 55 mA Max. 110 mA	–	–
MC 952 / 64 Mbytes / 5V Flash	6ES7952-1KY00-0AA0	Typ. 55 mA Max. 110 mA	–	–
Dimensions W x H x D W × H × D (in mm)		7,5 × 57 × 87		
Weight		Max. 35 g		
EMC protection		Provided by construction		

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